Proiectări VLSI

MN-211, 212

Oleg LUPAN, profesor univ., dr. hab.

D MIB, 3-429

Consultații

Miercuri 17-18

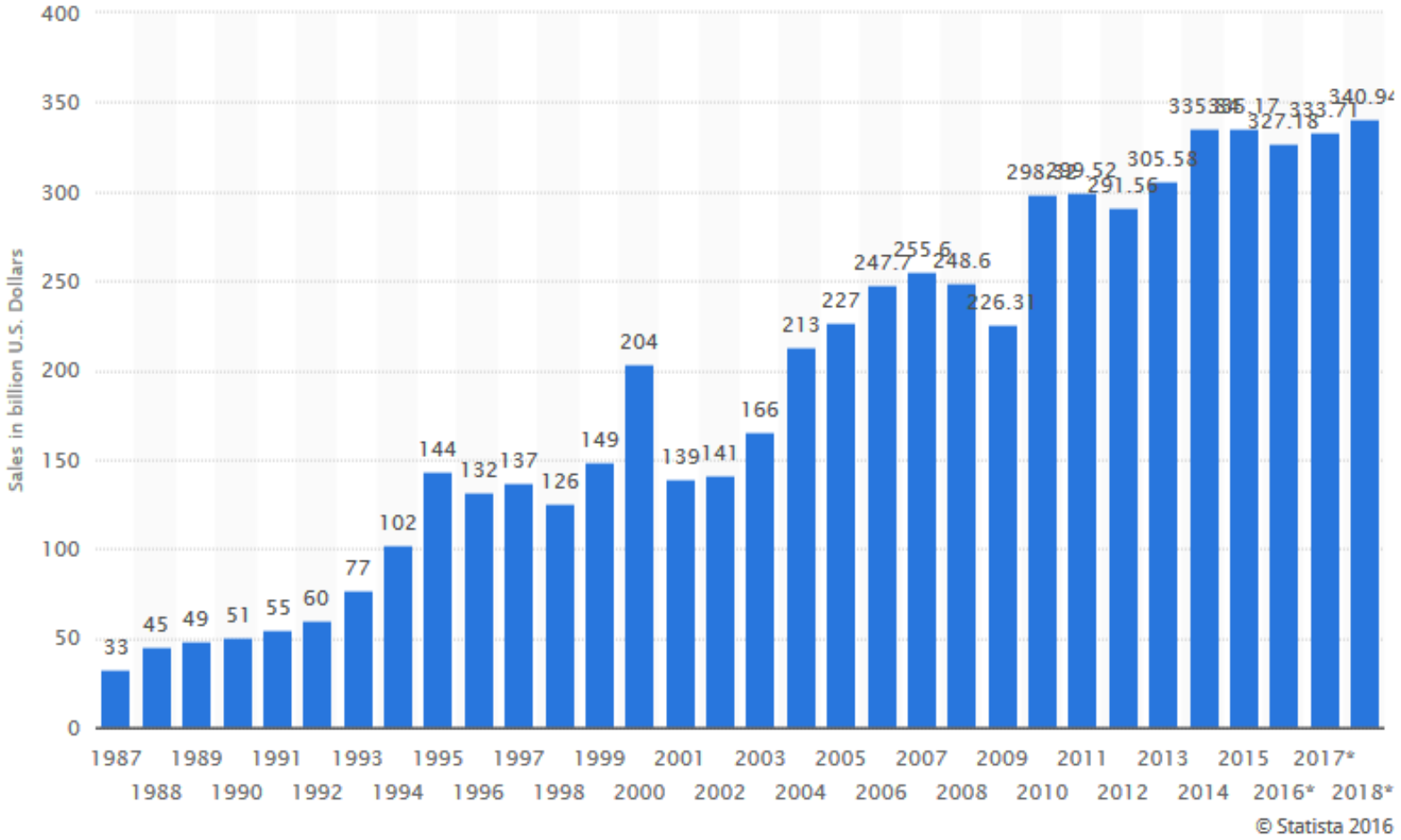
orice zi disponibila

Fabrication

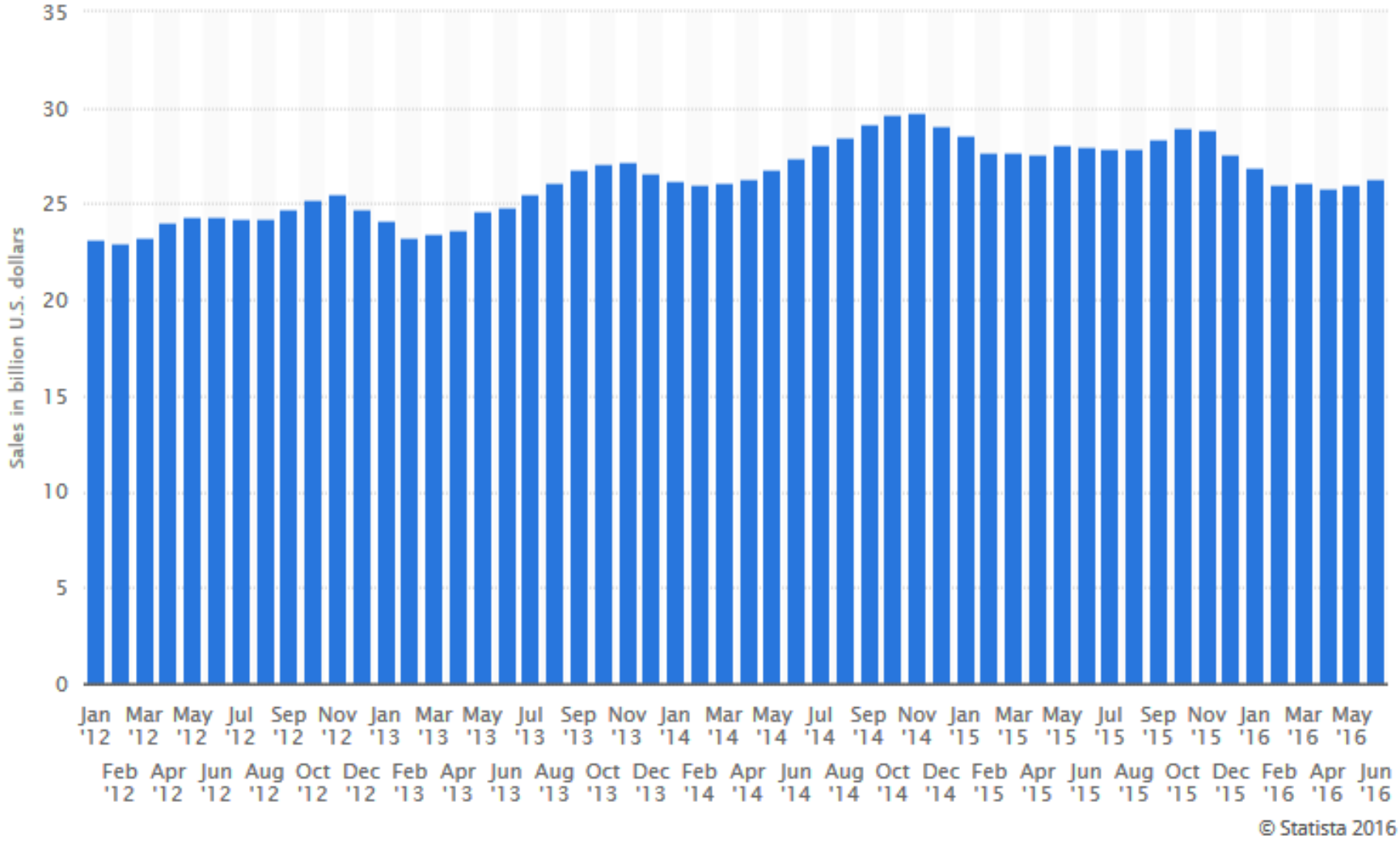
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

Examen

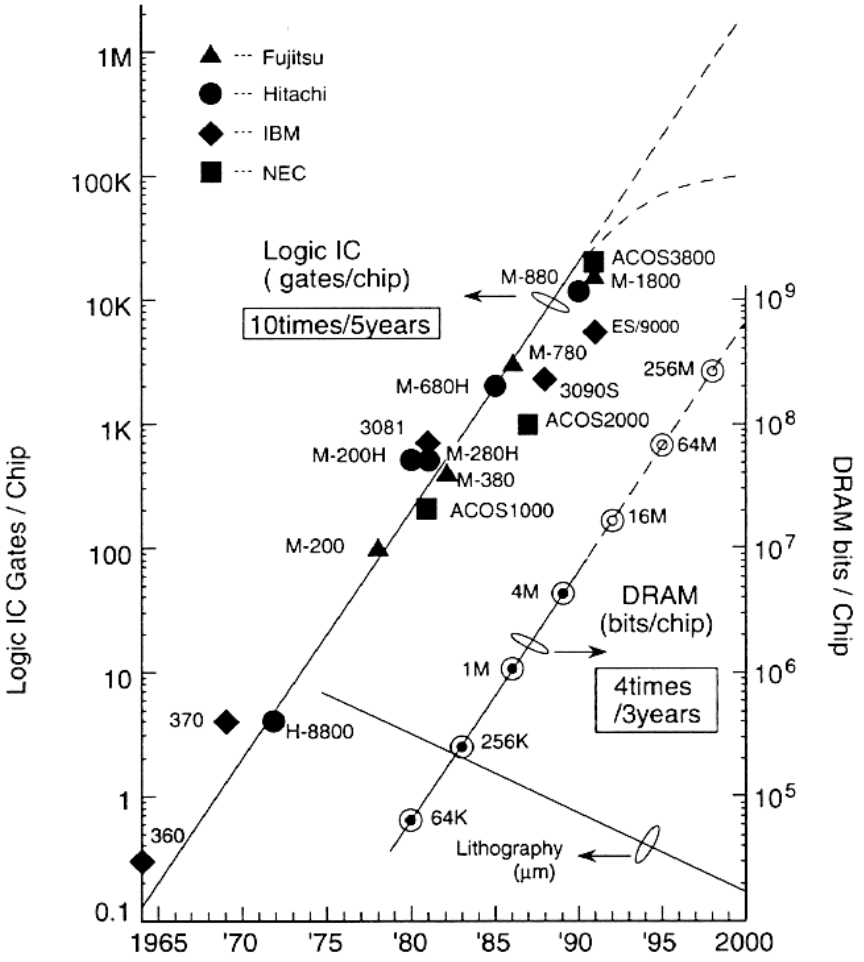
Pînă la 21 Decembrie 2024



www.statista.com



Evolution in Complexity



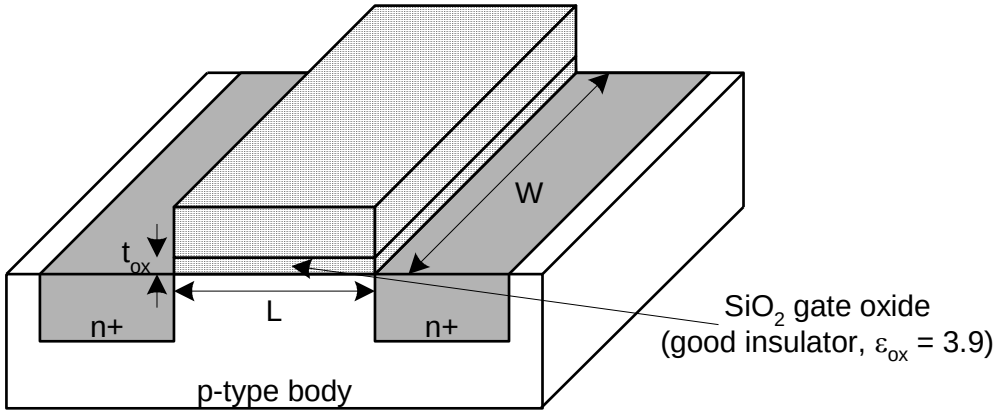
Capitolul 3.

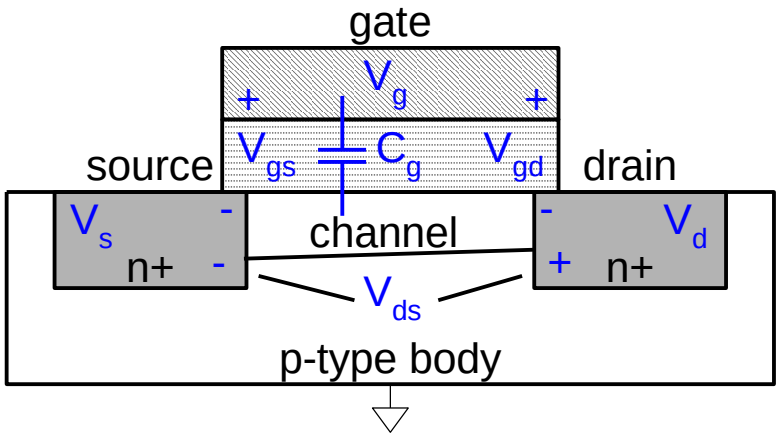
Proiectarea completa a mastilor de catre utilizator.

3.1 Introducere
3.2 Regulile de proiectare ale formelor CMOS .
3.3 Proiectarea formei inversorului CMOS .
Diagramele de bare
3.4 Forma portilor CMOS NAND si NOR .
3.5 Porti logice complexe CMOS .

Channel Charge

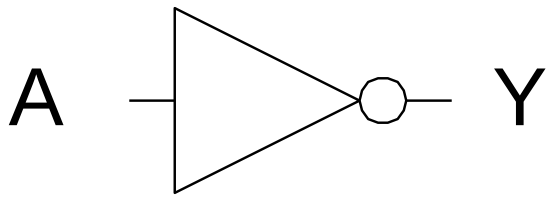
- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$ $\quad C_{ox} = \varepsilon_{ox} / t_{ox}$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

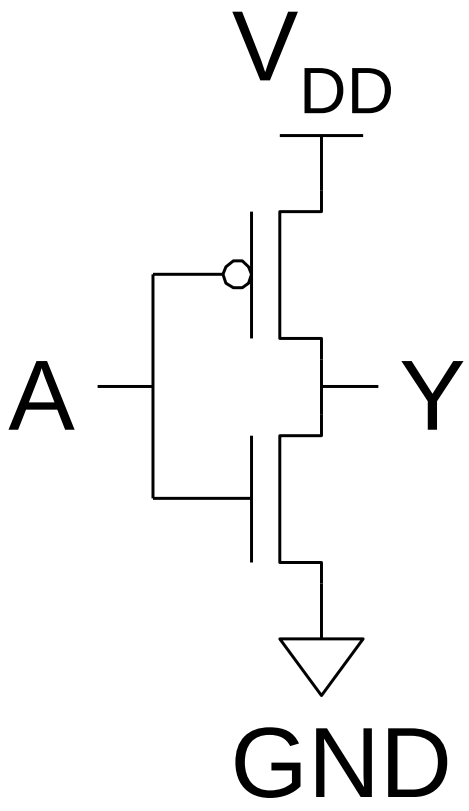




CMOS Inverter

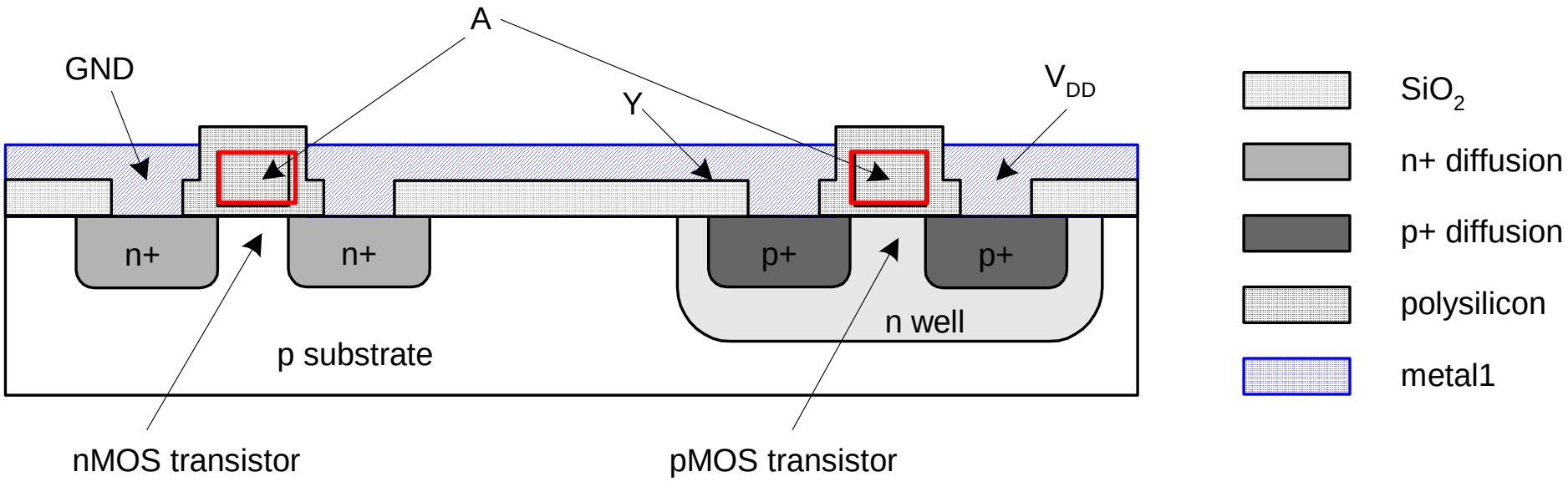
A	Y
0	
1	





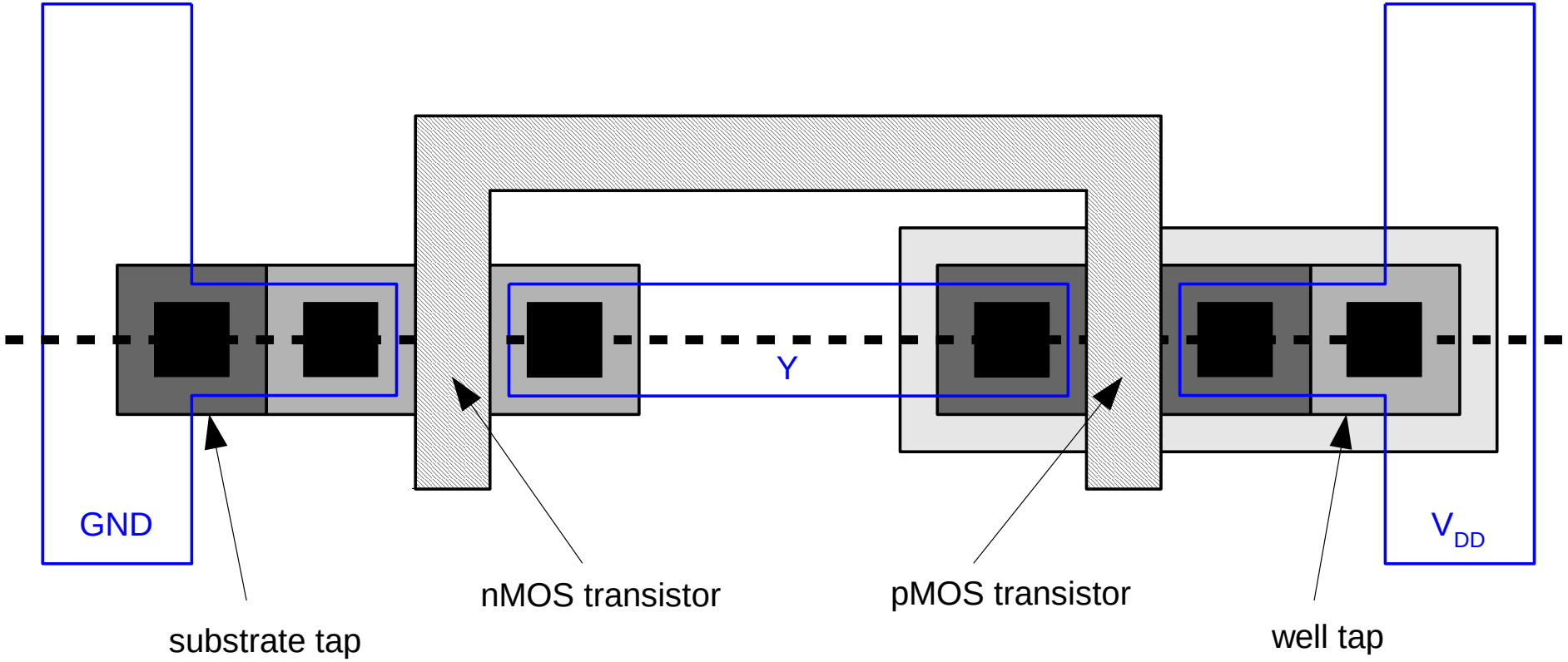
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



Inverter Mask Set

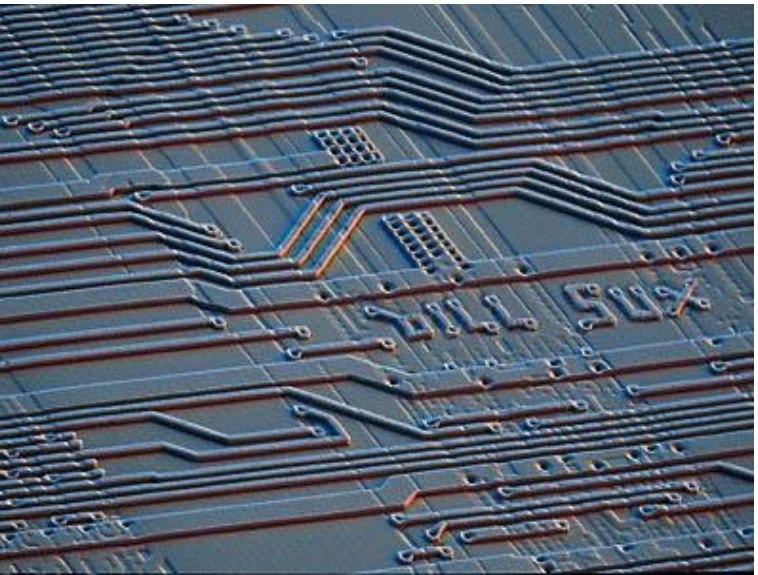
- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line

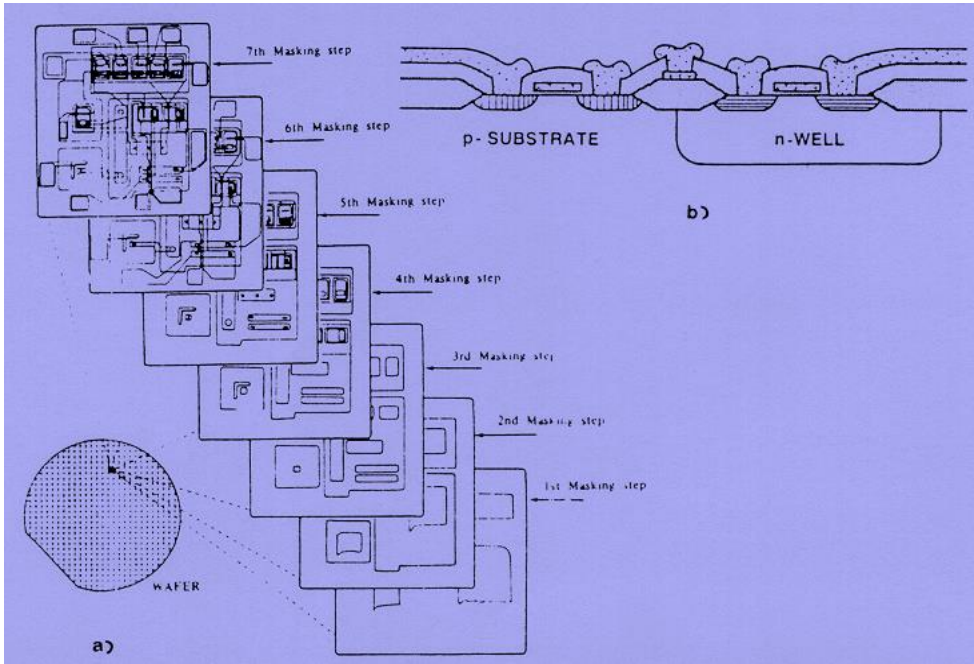


3.1 Introducere

În acest capitol vor fi prezentate ideile de baza pentru proiectarea mastilor.

Proiectarea mastilor fizice este foarte strâns legata de performanta generala
a circuitului (suprafata, viteza, putere disipata) intrucat structura fizica
determina direct
transductanta tranzistoarelor,
capacitatile parazite si rezistentele, si evident,
suprafata de siliciu, care este utilizata pentru o functie particulara.

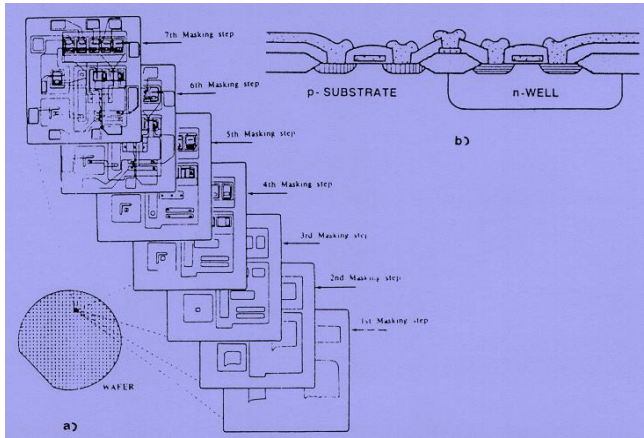




Pe de alta parte, proiectarea detaliata a mastilor necesita un efort intens si de durata, care este justificabil numai în situatiile in care suprafata si/sau performanta circuitului trebuie optimizate sub constrângeri stricte.

Prin urmare, generarea automata a mastii (de exemplu celule standard + plasamentul si conectarea asistate de calculator) este în mod obisnuit preferata pentru proiectarea majoritatii circuitelor digitale VLSI.

Totusi, pentru a aprecia restrictiile fizice, cat si limitarile, proiectantii VLSI trebuie, de asemenea, sa posede o buna întelegere a procesului fizic de realizare a mastilor.



Desenarea mastilor trebuie sa satisfaca strict cu un set de reguli de proiectare, cum sunt cele descrise în capitolul 2.

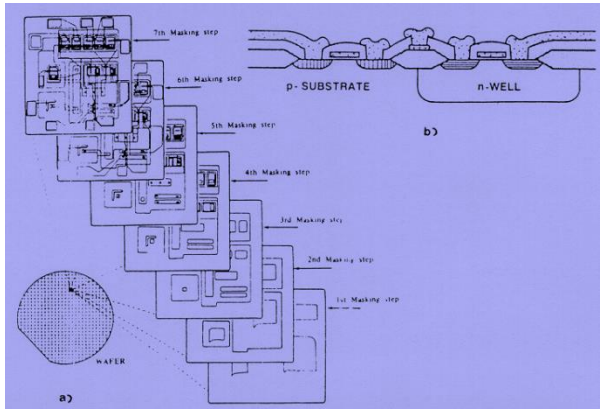
In consecinta, acest capitol va incepe cu examinarea unui set complet de reguli de proiectare. Proiectarea unui inversor simplu CMOS va fi prezentata pas cu pas, pentru a arata influenta numeroaselor reguli asupra structurii mastii si asupra dimensiunilor.
De asemenea, se va introduce un concept de diagrame de bare, care pot fi utilizate eficient pentru simplificarea topologiei generale a mastilor în fazele incipiente ale proiectarii.

Cu ajutorul diagramelor de bare, proiectantul poate intelege mai bine restrictiile topologice si poate testa rapid mai multe posibilitati pentru a gasi forma optima, fara a desena diagrama completa a mastii.

Proiectarea mastilor portilor logice CMOS este un proces iterativ, care începe cu topologia circuitului (pentru a realiza functia logica dorita) si dimensionarea initiala a tranzistoarelor (pentru a realiza specificatiile legate de performanta).

În acest punct, proiectantul poate numai sa estimeze încarcarea capacitiva parazita totala la nodul de iesire, bazat pe: fan-out, numarul de dispozitive si lungimea anticipata a liniilor de interconexiune.

Daca poarta logica contine mai mult de 4-6 tranzistoare, reprezentarea topologiei grafului si metoda caii Euler permit proiectantului sa determine ordonarea optima a tranzistoarelor. Se poate trasa o forma simpla a diagramei de bare, aratând amplasarea tranzistoarelor, interconexiunile locale dintre tranzistoare si asezarea contactelor.



Dupa gasirea unei forme fezabile, din punct de vedere topologic, sunt trasate mastile diferitelor straturi (folosind unelte de editare a mastilor/formelor geometrice) în concordanta cu regulile de proiectarea ale acestora.

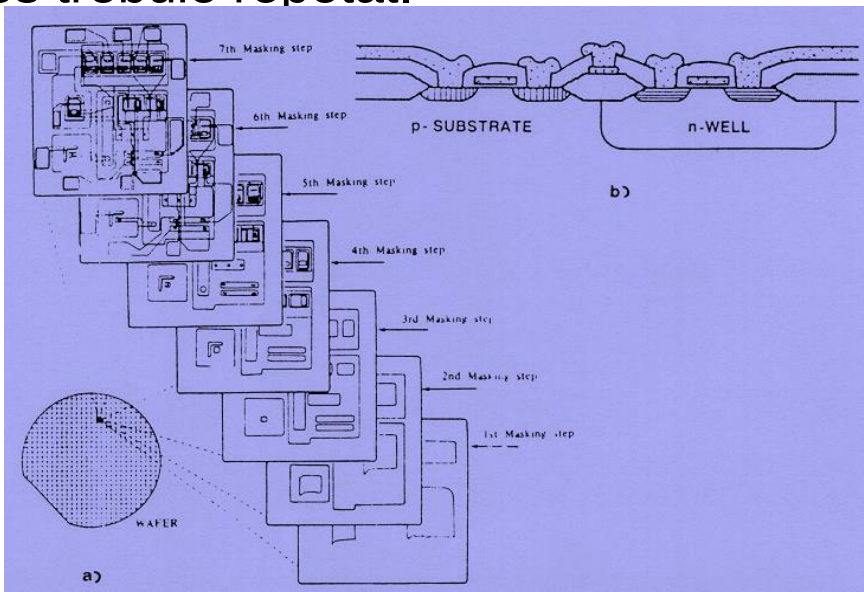
Aceasta procedura poate necesita mai multe iteratii pentru a satisface toate regulile de proiectare, in schimb topologia de baza nu se va modifica în mod semnificativ.

Dupa verificarile finale are regulilor de proiectare (DRC – Design Rule Check), se executa o procedura de extragere a circuitului, din mastile finale, pentru a determina dimensiunile reale ale tranzistoarelor, si in special, capacitatile parazite în fiecare nod.

Rezultatul pasului de extragere este în mod obisnuit un fisier detaliat de intrare SPICE, fisier care este în mod automat generat de uneltele de extragere.

În acest moment, performanta curenta a circuitului poate fi determinata prin folosirea unei simulari SPICE, folosind lista nodurilor extrase.

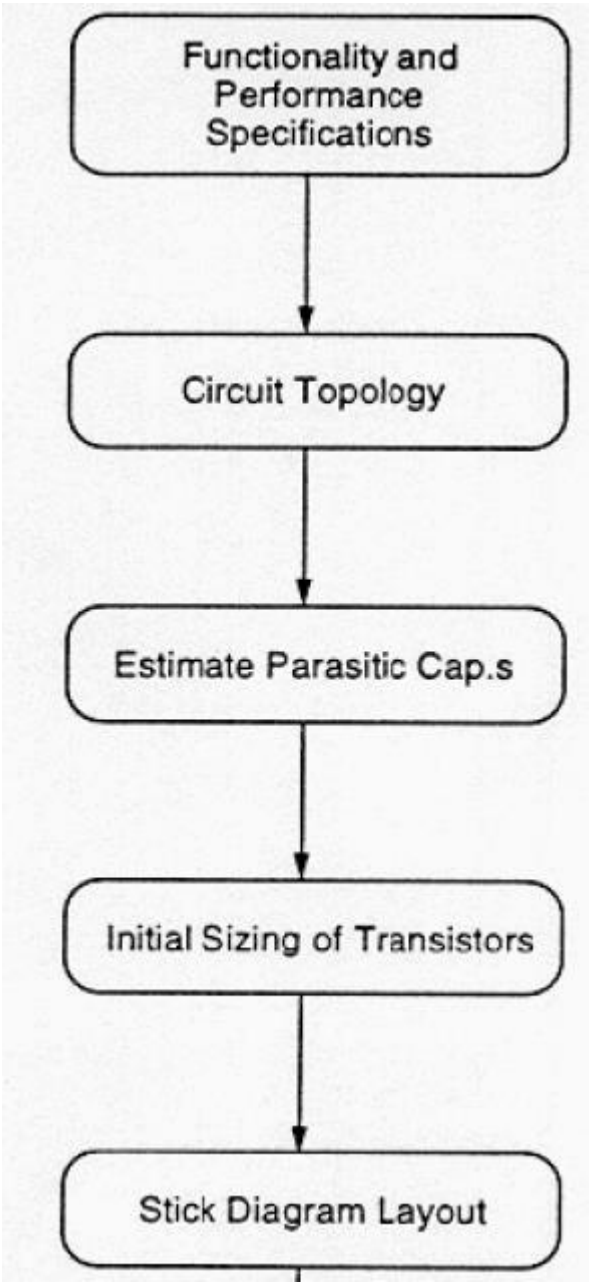
Daca performanta circuitului simulat (de exemplu timpul de raspuns tranzitoriu sau puterea disipata) nu satisface specificatiile dorite, mastile trebuie modificate si întregul proces trebuie repetat.



Modificarile mastilor se refera în mod obisnuit la raportul W/L (latime/lungime) al tranzistoarelor (redimensionarea tranzistoarelor), intrucat acest raport determina transductanta si capacitatile parazite ale sursei si drenei.

Proiectantul poate, de asemenea, decide sa schimbe o parte sau intreaga topologie a circuitului pentru a reduce elementele parazite.

Diagrama acestui proces iterativ este prezentata în figura 3.1.



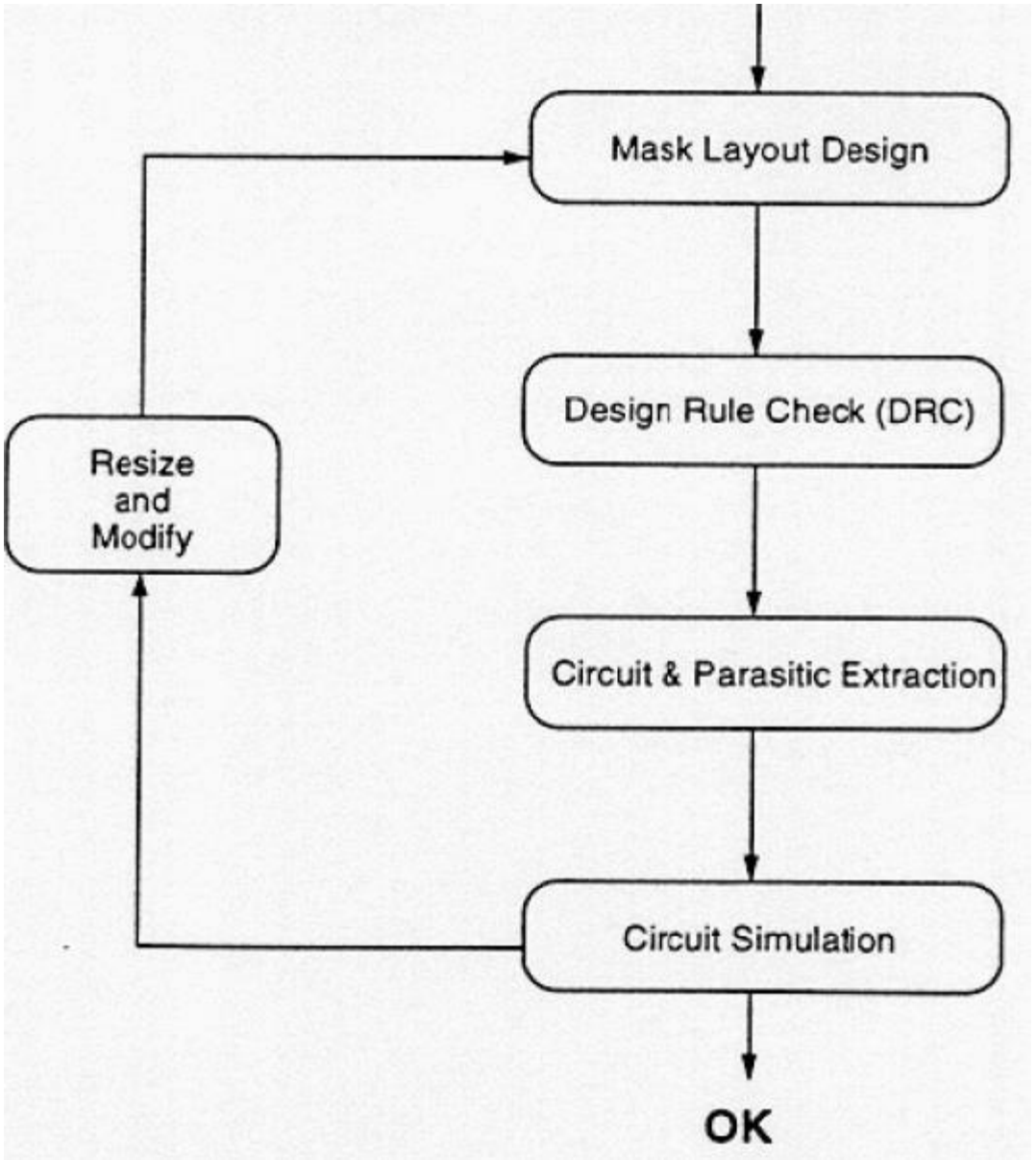


Figura 3.1: Fluxul obisnuit de proiectare pentru realizarea unei masti.

Design VLSI

Fabrication

3.2 Regulile de proiectare ale formelor CMOS

Asa cum s-a discutat în capitolul 2, fiecare proiect privind mastile trebuie sa se conformeze unui set de reguli de reguli, care dicteaza restrictiile geometrice impuse pentru masti, de catre tehnologia si de procesul de fabricatie.

Proiectantul formei trebuie sa se conformeze acestor reguli pentru a garanta o anumita calitate a produsului final, de exemplu, un anumit raport acceptabil de circuite defecte scoase de pe banda de fabricatie.

Un proiect care încalca unele dintre reguli poate totusi duce la un circuit functional; este de asteptat o calitate mai scazuta, datorita variatiilor aleatoare ale procesului.

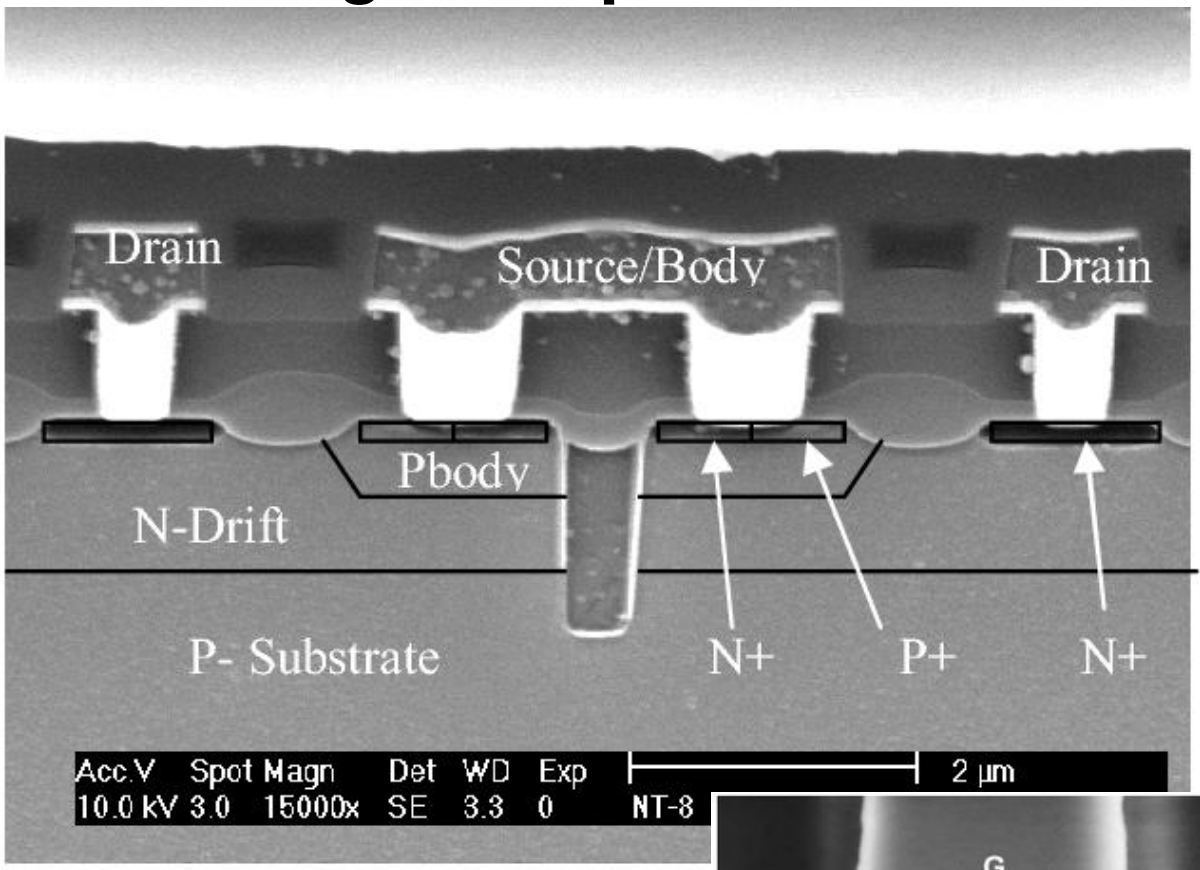
Regulile de proiectare de mai jos sunt date în termeni de reguli scalabile lambda.

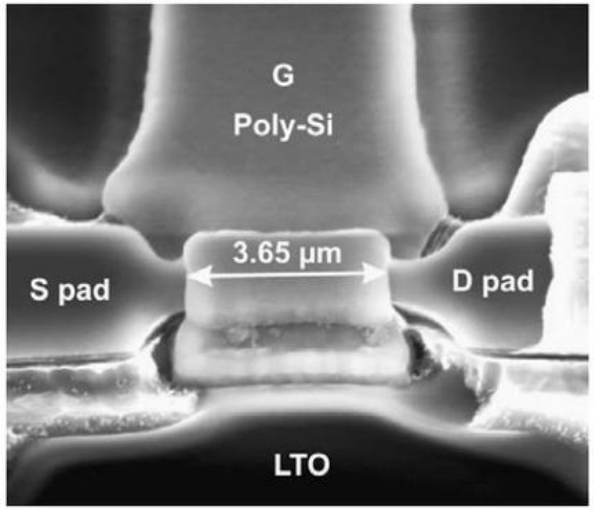
Trebuie remarcat ca, în timp ce regulile de proiectare scalabile sunt foarte utile pentru definirea unor masti independente de tehnologia folosita si pentru a satisface constrângerile de baza, cele mai multe reguli nu se scaleaza liniar, în special pentru tehnologiile submicronice.

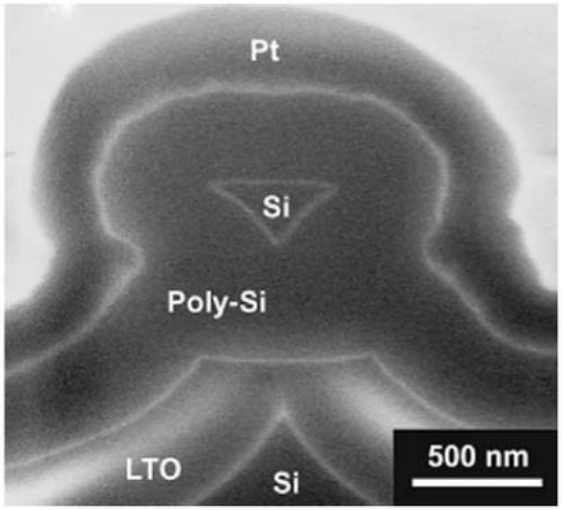
Prin urmare, regulile de proiectare lambda nu sunt utile pentru tehnologiile CMOS submicronice.

All paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process.

2.5 Reguli de proiectare.

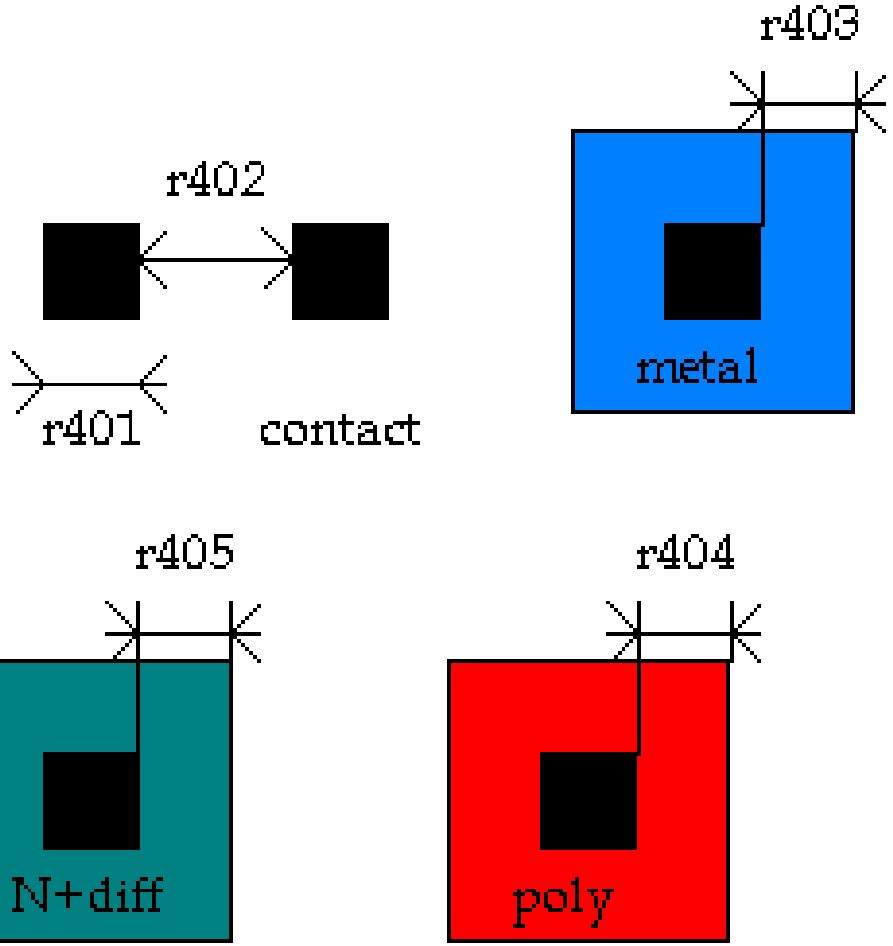






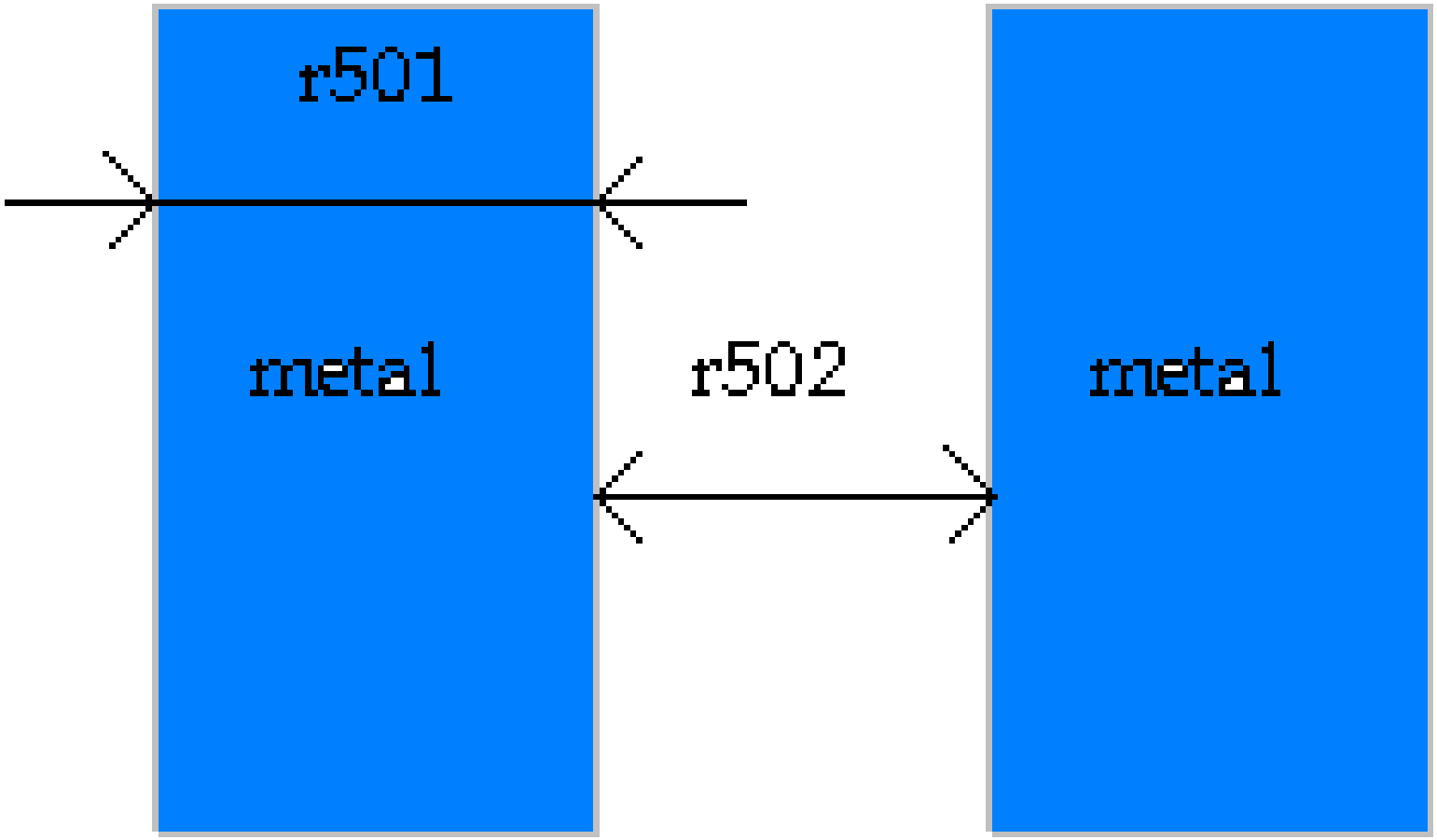
Contact.

- r401 latimea contactului: 2
- r402 distanta minima intre doua contacte: 3
- r403 extensia metalului fata de taietura de contact: 2
- r404 extensia siliciului policristalin fata de taietura de contact: 2
- r405 extensia difuziei fata de taietura de contact: 2



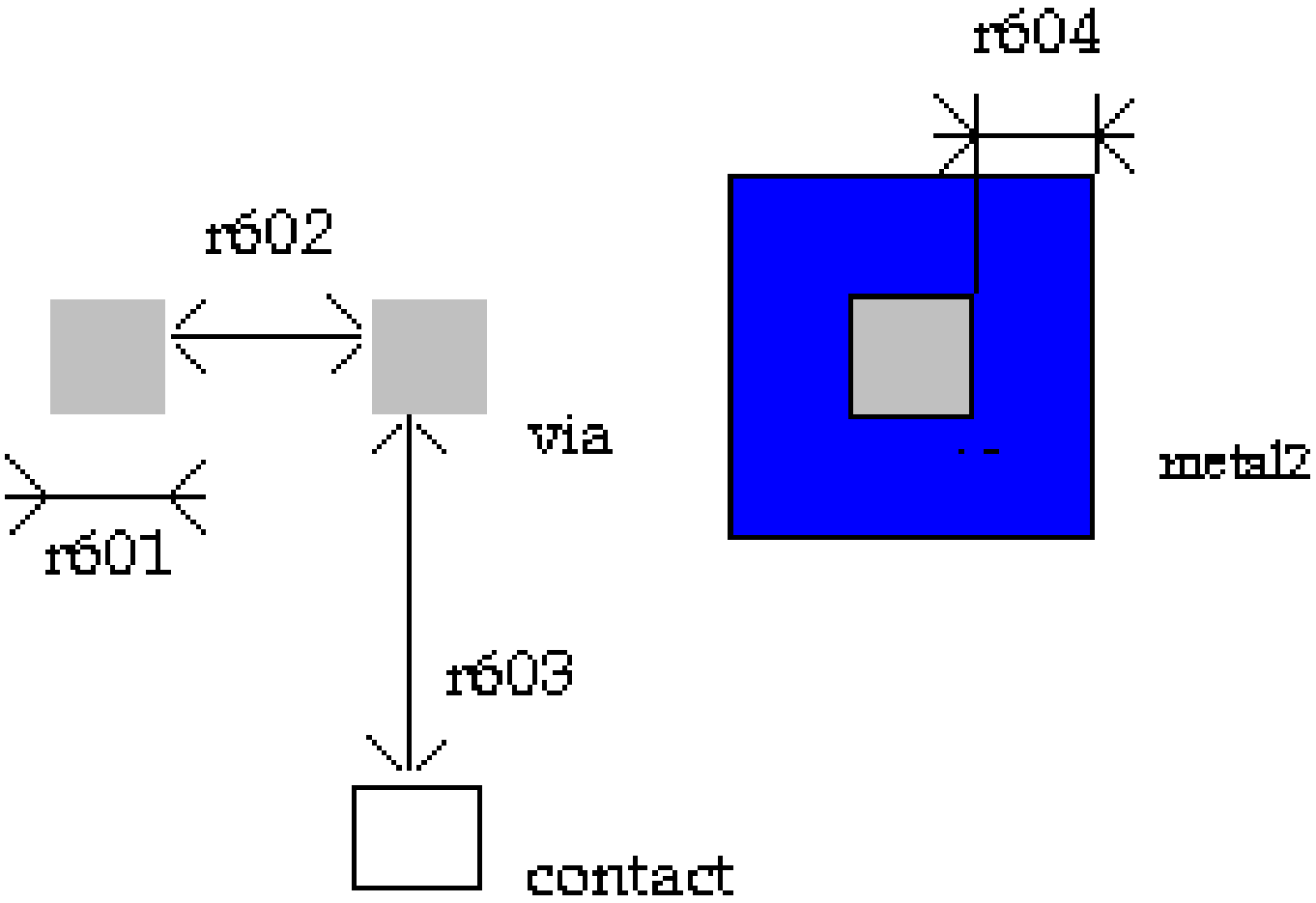
Metal1

- r501 dimensiunea minima a metalului1: 3
- r302 distanta minima intre doua zone de metal1: 3



Via.

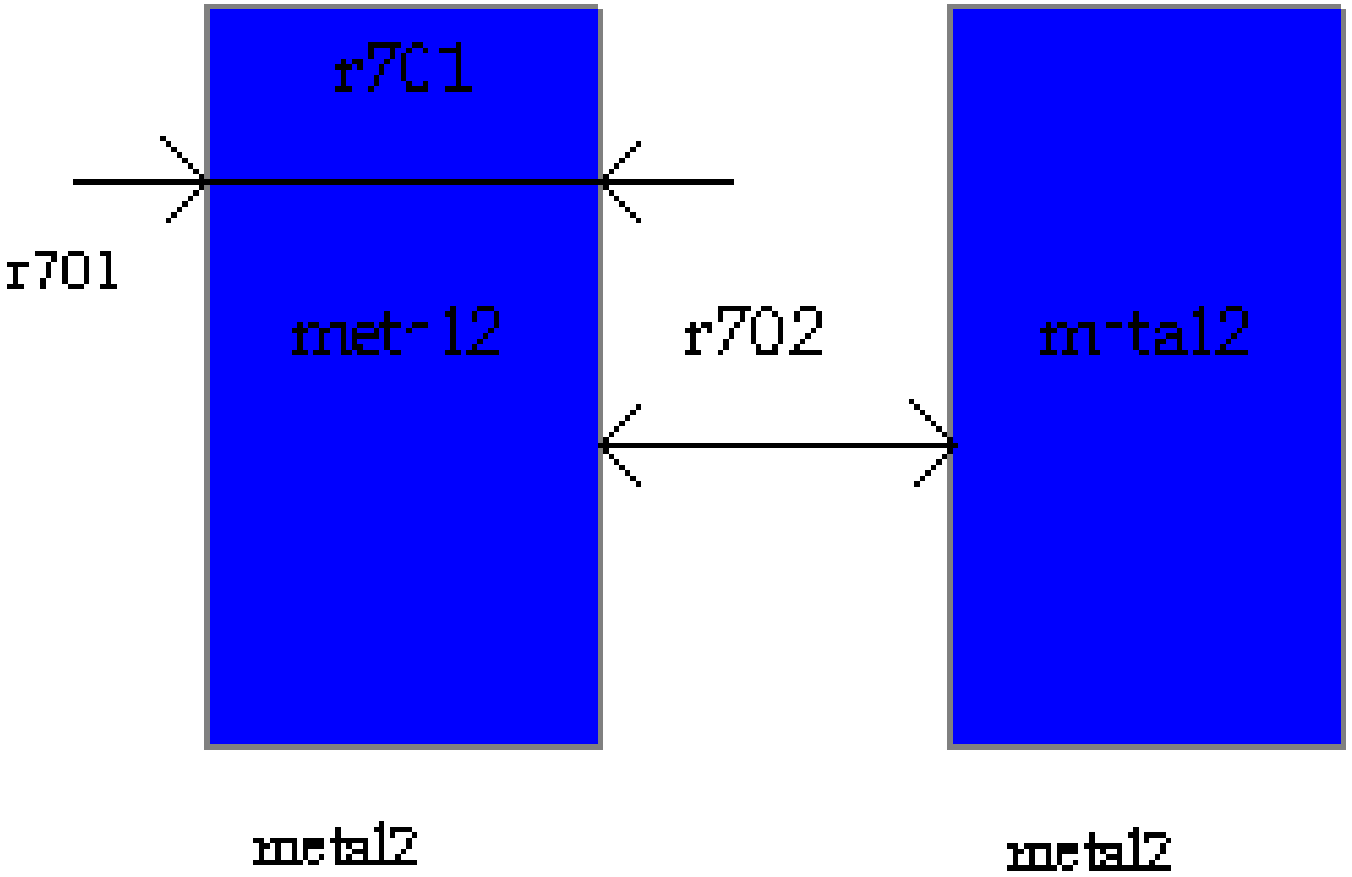
- r601 latimea zonei via: 3
- r602 distanta minima intre doua zone via: 3
- r603 distanta minima intre via si contact: 3
- r604 extensia metal1 peste via: 2
- r605 extensia metal2 peste via: 2



Metal2.

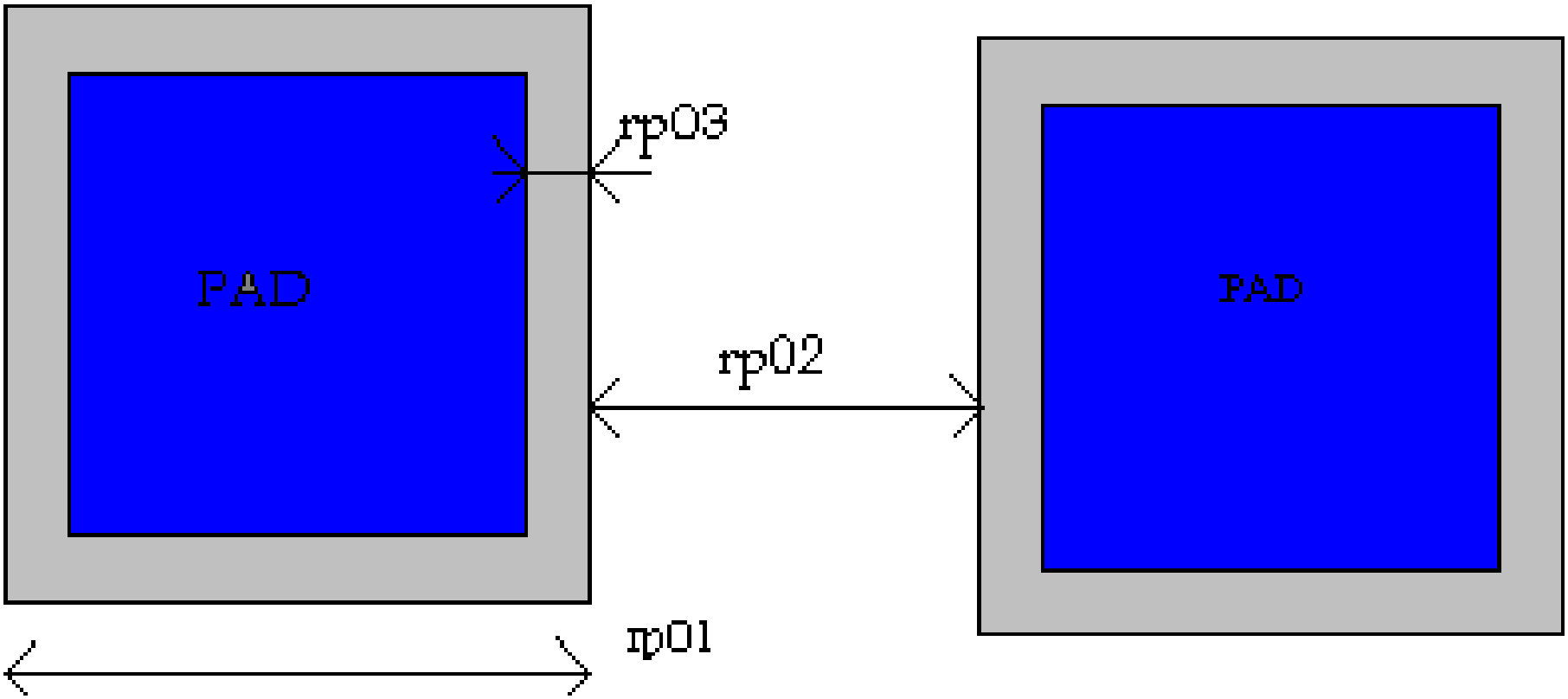
• r701 dimensiunea minima a zonei de metal2: 5

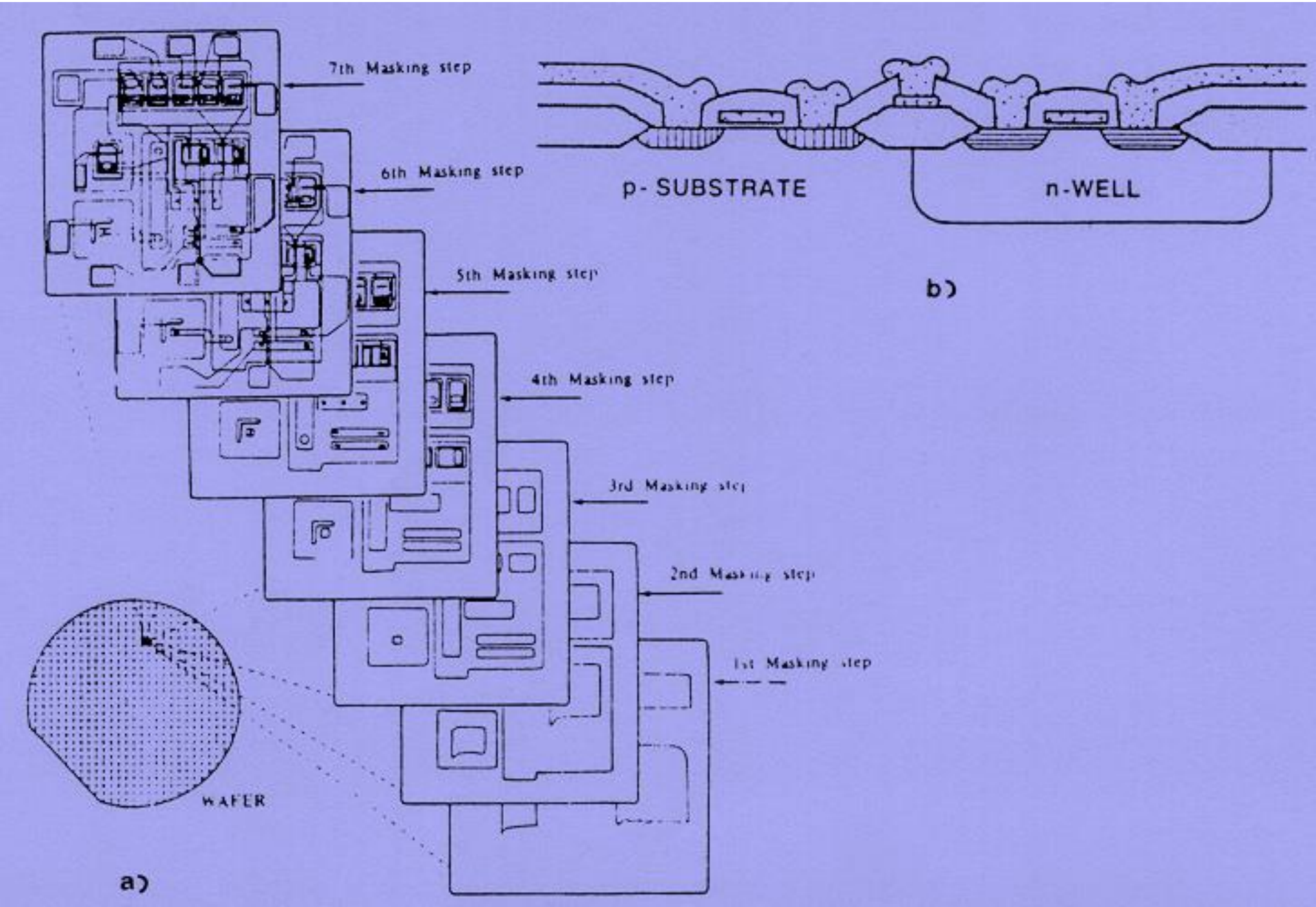
• r702 distanta minima intre doua zone de metal2: 5

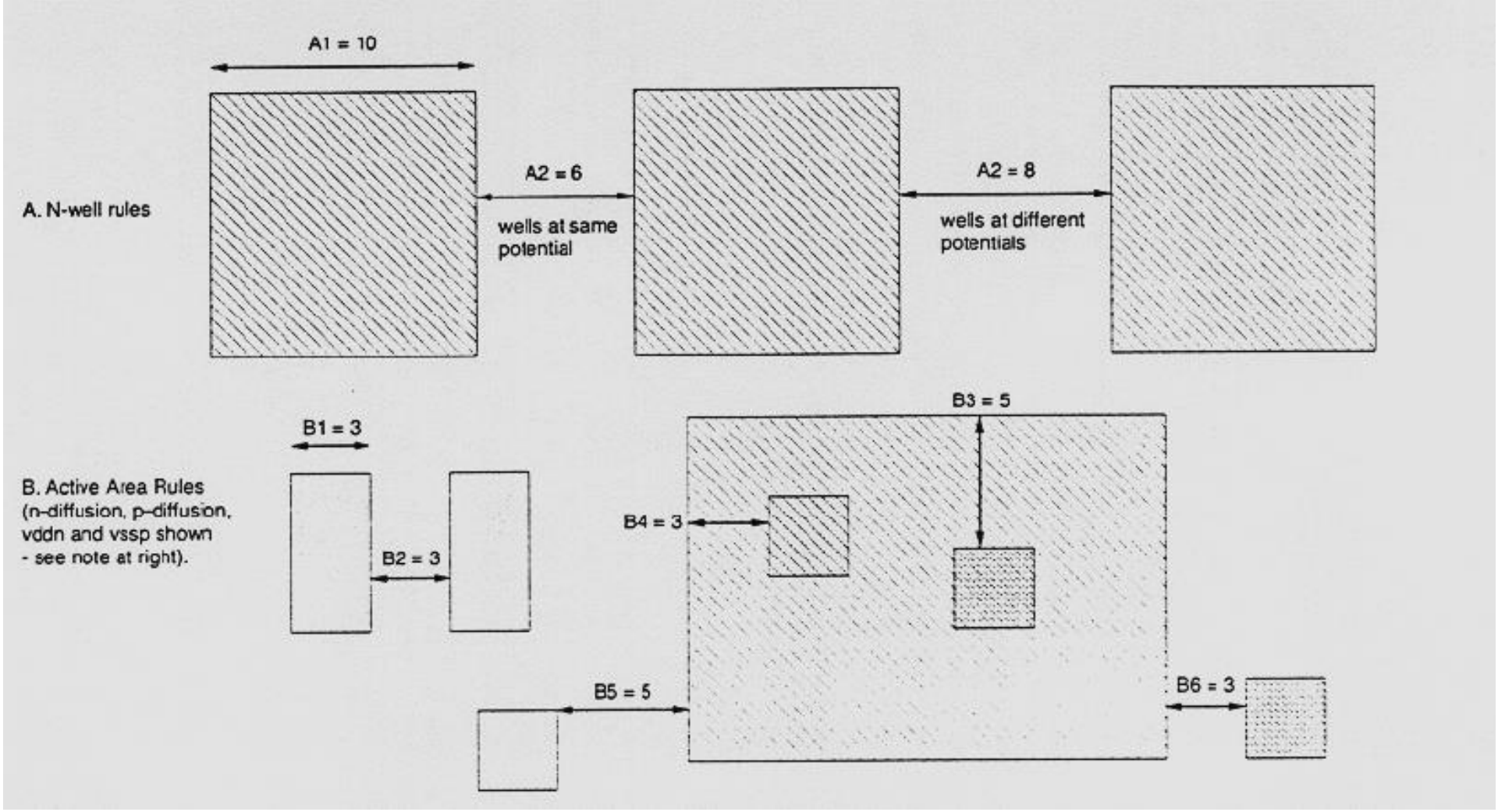


Plotul

- rp01 dimensiunea minima 100 µm
- rp02 distanta minima intre doua ploturi: 100 µm




7th Masking step
6th Masking step
5th Masking step
4th Masking step
3rd Masking step
2nd Masking step
1st Masking step
WAFER
a)
p- SUBSTRATE
n-WELL
b)



24.10.2024

Figura 3.2: Ilustrarea unor reguli de proiectare a mastilor CMOS

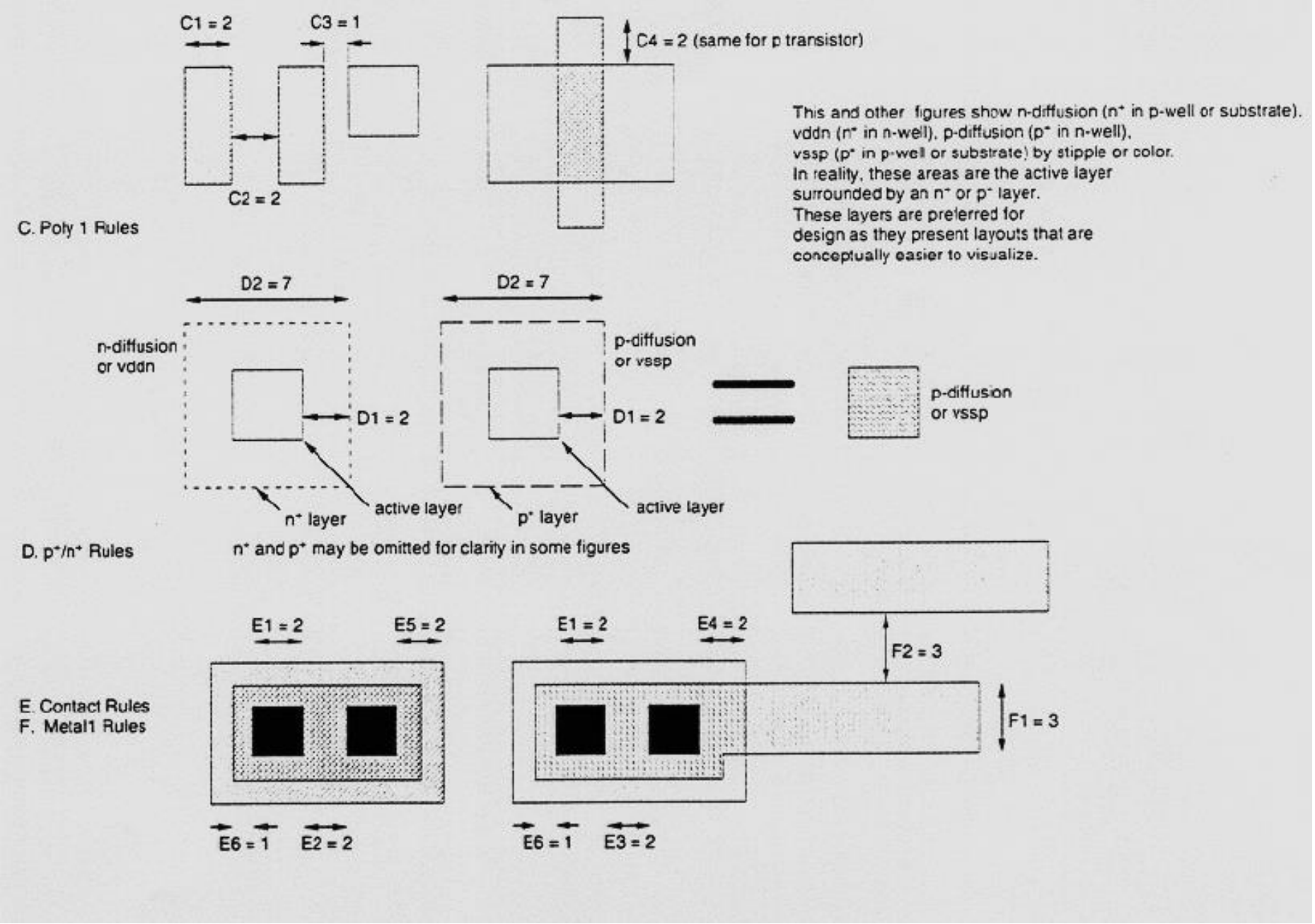


Figura 3.2: Ilustrarea unor reguli de proiectare a mastilor CMOS

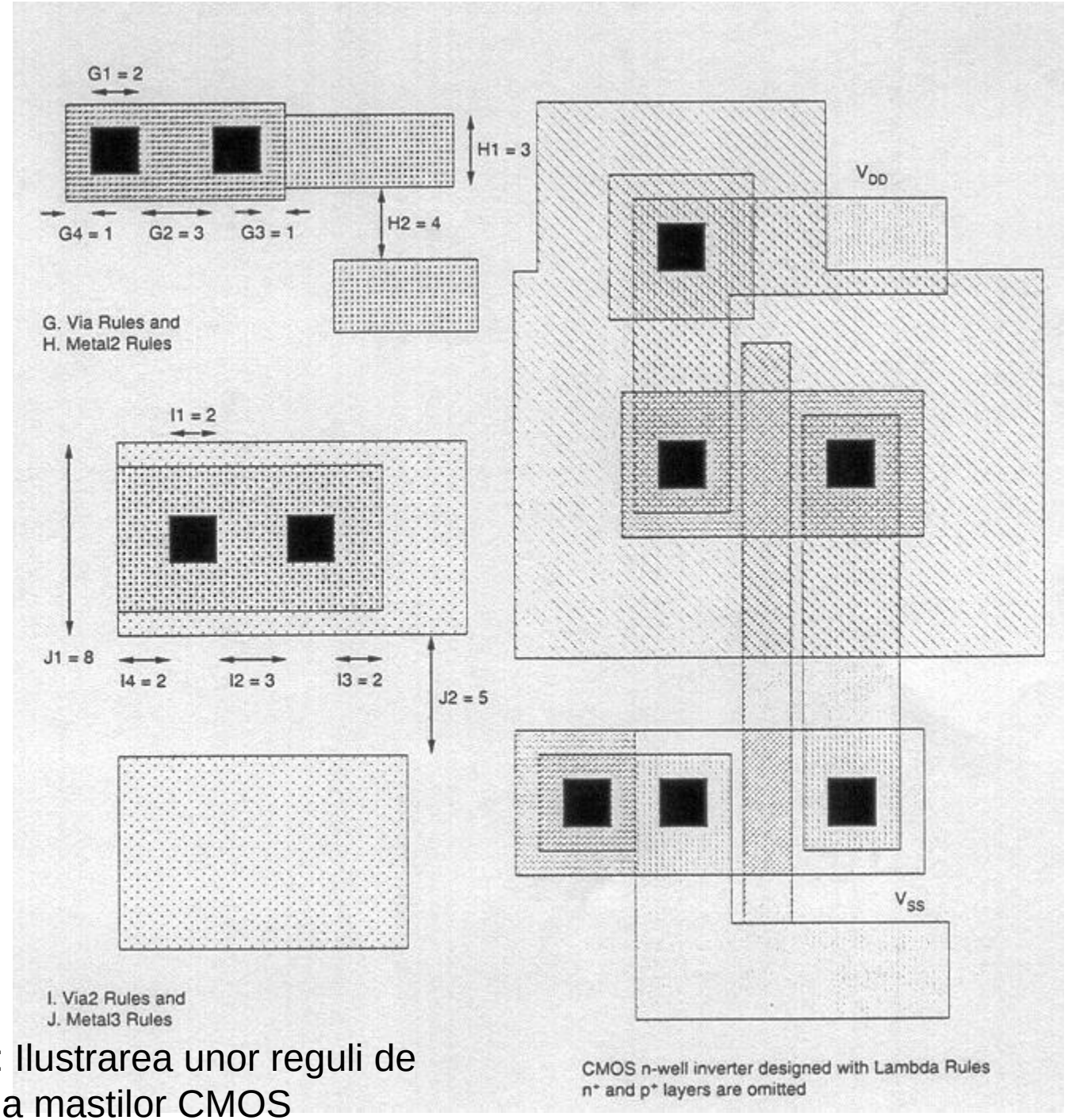
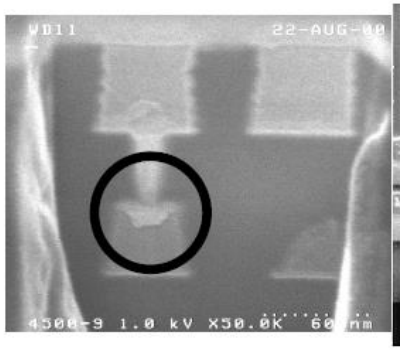
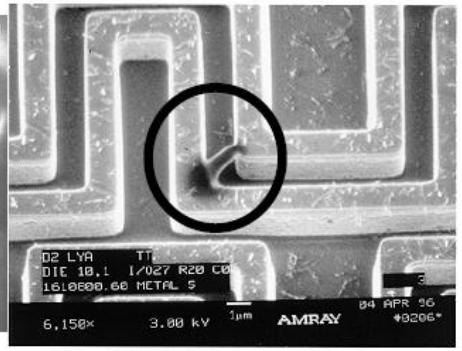


Figura 3.2: Ilustrarea unor reguli de proiectare a mastilor CMOS

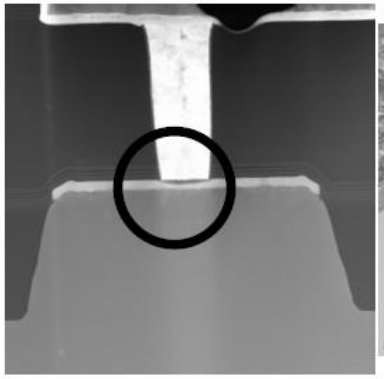
Manufacturing Failures



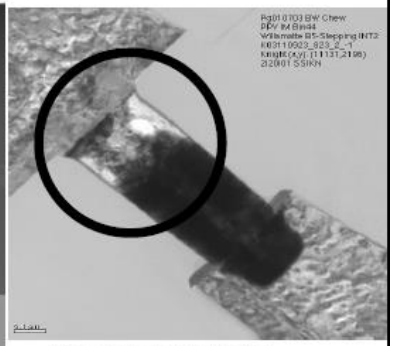
Metal 1 Shelving



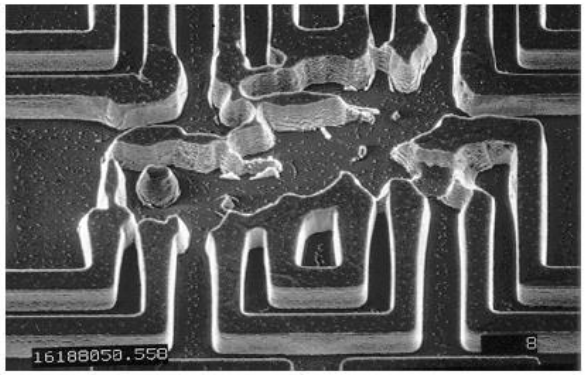
Metal 5 film particle
(bridging defect)



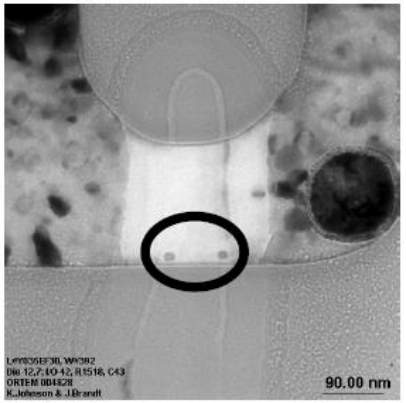
Open defect



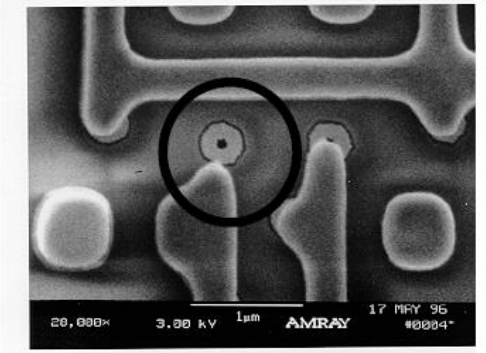
Spongy Via2
(Infant mortality)



Metal 5 blocked etch
(patterning defect)



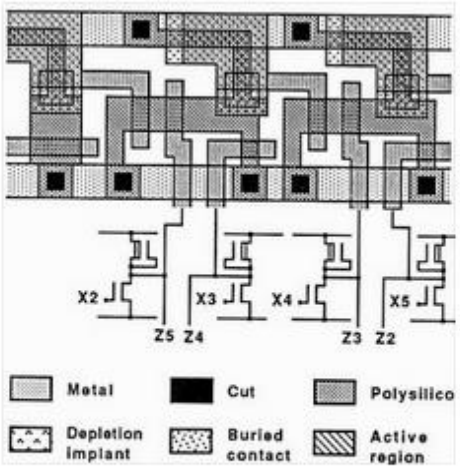
Spot defects
"Co" Defect under Gate



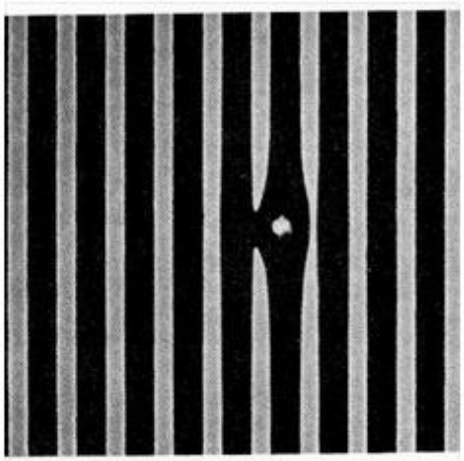
Metal 1 missing pattern
(open at contact)

SEM images courtesy Intel Corporation

Manufacturing Failures

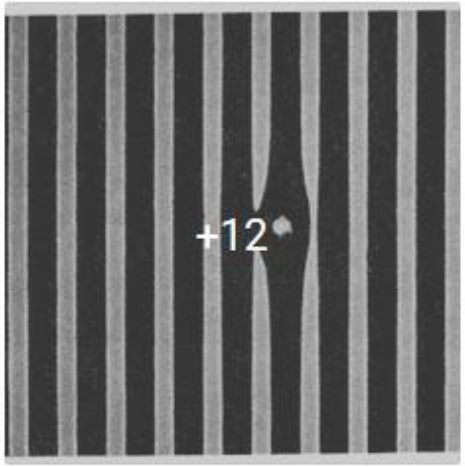


Example of metal line corrosion that eventually may result in break...



Example of a break in a metal line.

Example of a break of 7 metal lines caused by the interaction bet...

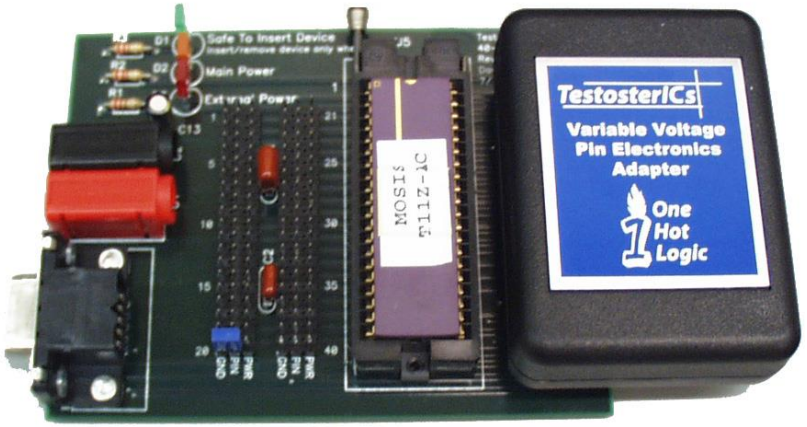


depicts the spat defect formed by a very typical mechanism in whi...

SEM images courtesy Intel Corporation

TestosterICs

- TestosterICs functional chip tester
  - Designed by clinic teams and David Diaz at HMC
  - Reads your test vectors, applies them to your chip, and reports assertion failures



3.3 Proiectarea formei inversorului CMOS . Diagramele de bare .

În continuare se va examina pas cu pas proiectarea mastilor unui inversor CMOS.

Circuitul consta intr-un tranzistor nMOS si unul pMOS, prin urmare, unii pot presupune ca topologia formei este relativ simpla.

Se va vedea ca exista un numar destul de mare de posibilitati de proiectare chiar si pentru un circuitatat de simplu.

În primul rând, trebuie sa fie create tranzistoarele individuale în concordanta cu regulile de proiectare.

Se presupune ca se va încerca sa se proiecteze un inversor cu tranzistoare de dimensiuni minime.

Latimea suprafetei active este apoi determinata de dimensiunea minima a contactului zonei de difuzie (pentru conexiunile sursa si drena) si separarea minima dintre contactul de difuzie si ambele margini ale suprafetei active.

Latimea liniei de siliciu policristalin, peste suprafa activa, (poarta tranzistorului) este în mod obisnuit luata ca latimea „poli” minima (figura 3.3).

Apoi, lungimea totala a suprafetei active este determinata simplu de urmatoarea suma: (latimea „poli” minima) + 2.(distanta minima dintre „poli” si contact) + 2.(distanta minima dintre contact si marginile suprafetei active).

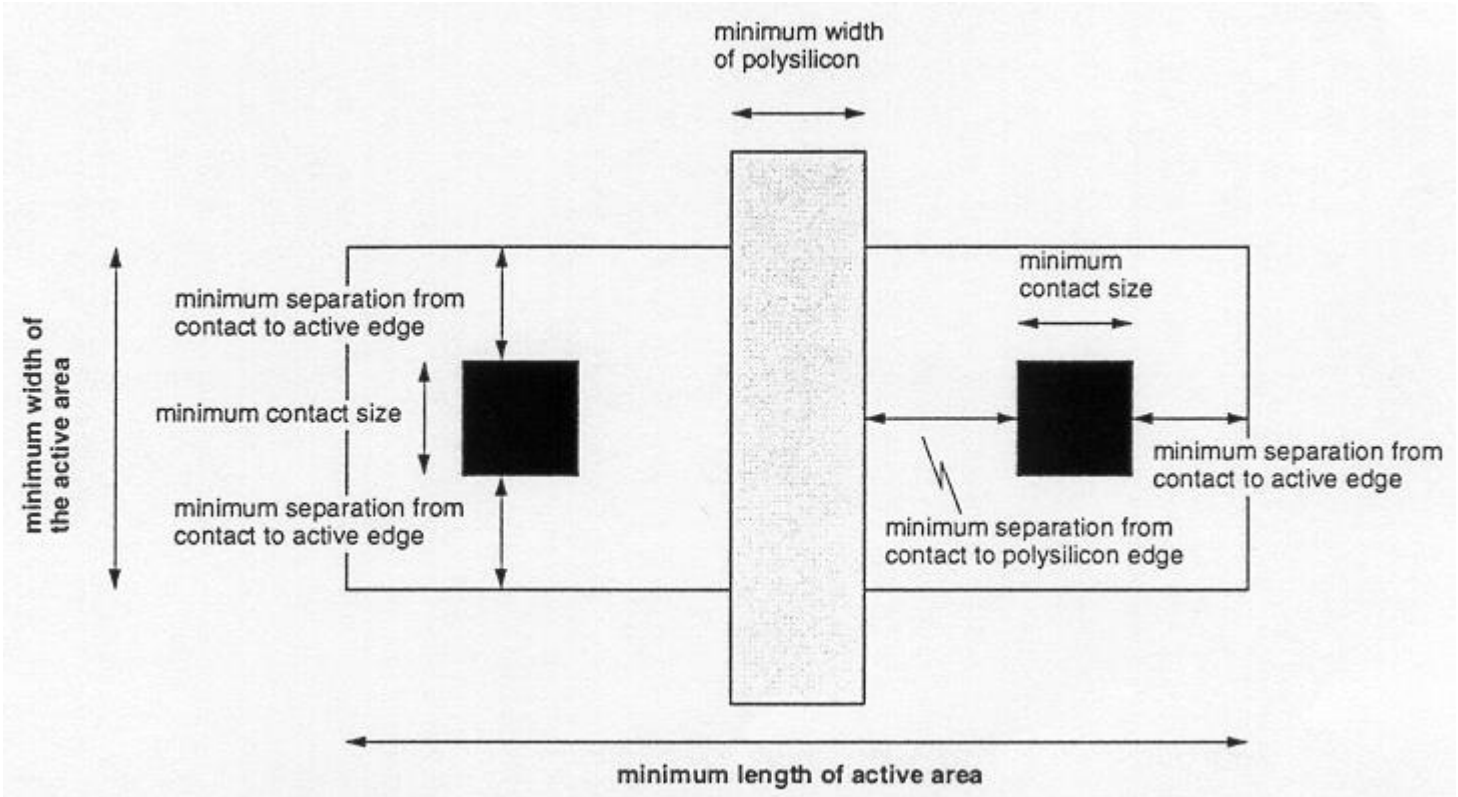
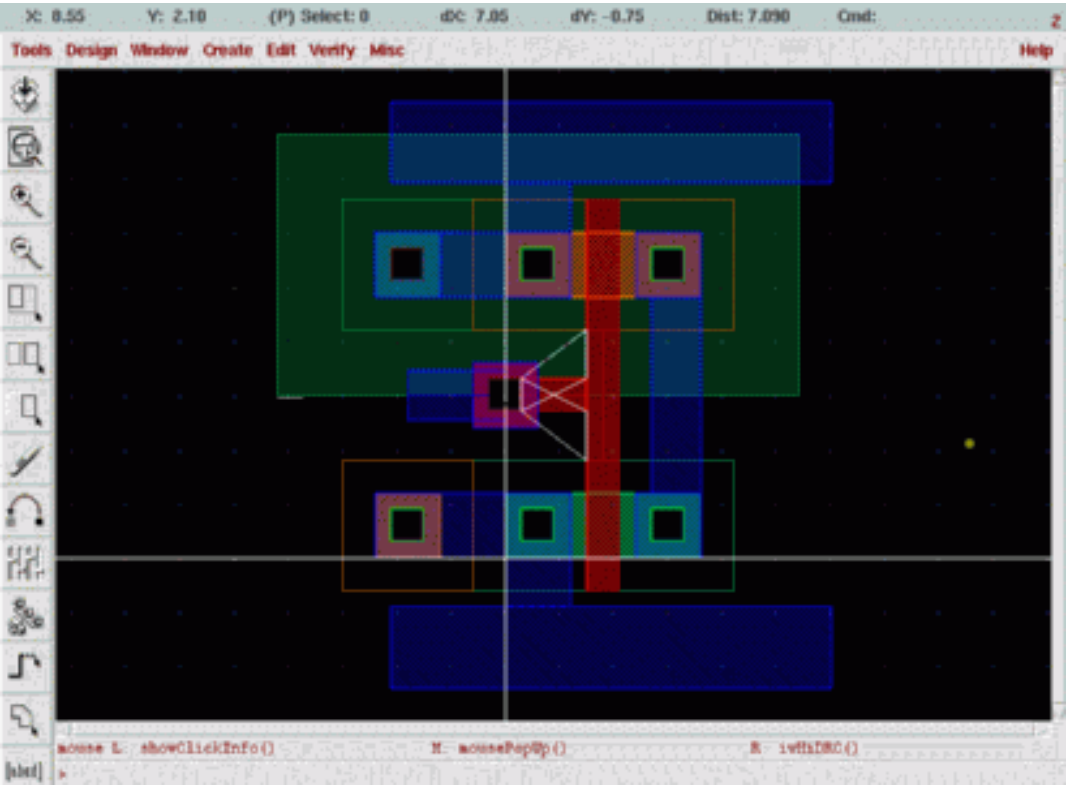


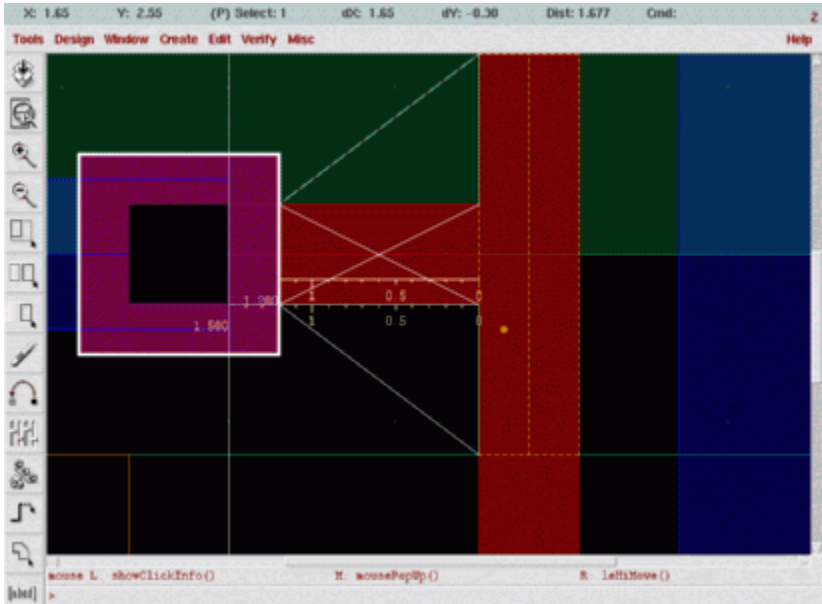
Figura 3.3: Restrictiile regulilor de proiectare, care determina dimensiunea unui tranzistor de marime minima

Tranzistorul pMOS trebuie plasat pe o insula n, dimensiunea minima a acestei insule fiind dictata de suprafata activa pMOS si de extinderea minima a acesteia peste zona p+.

Dinstanta dintre tranzistoarele nMOS si pMOS este determinata de separarea minima dintre suprafata activa n+ si insula n (figura 3.4).

The errors are also highlighted on the layout.





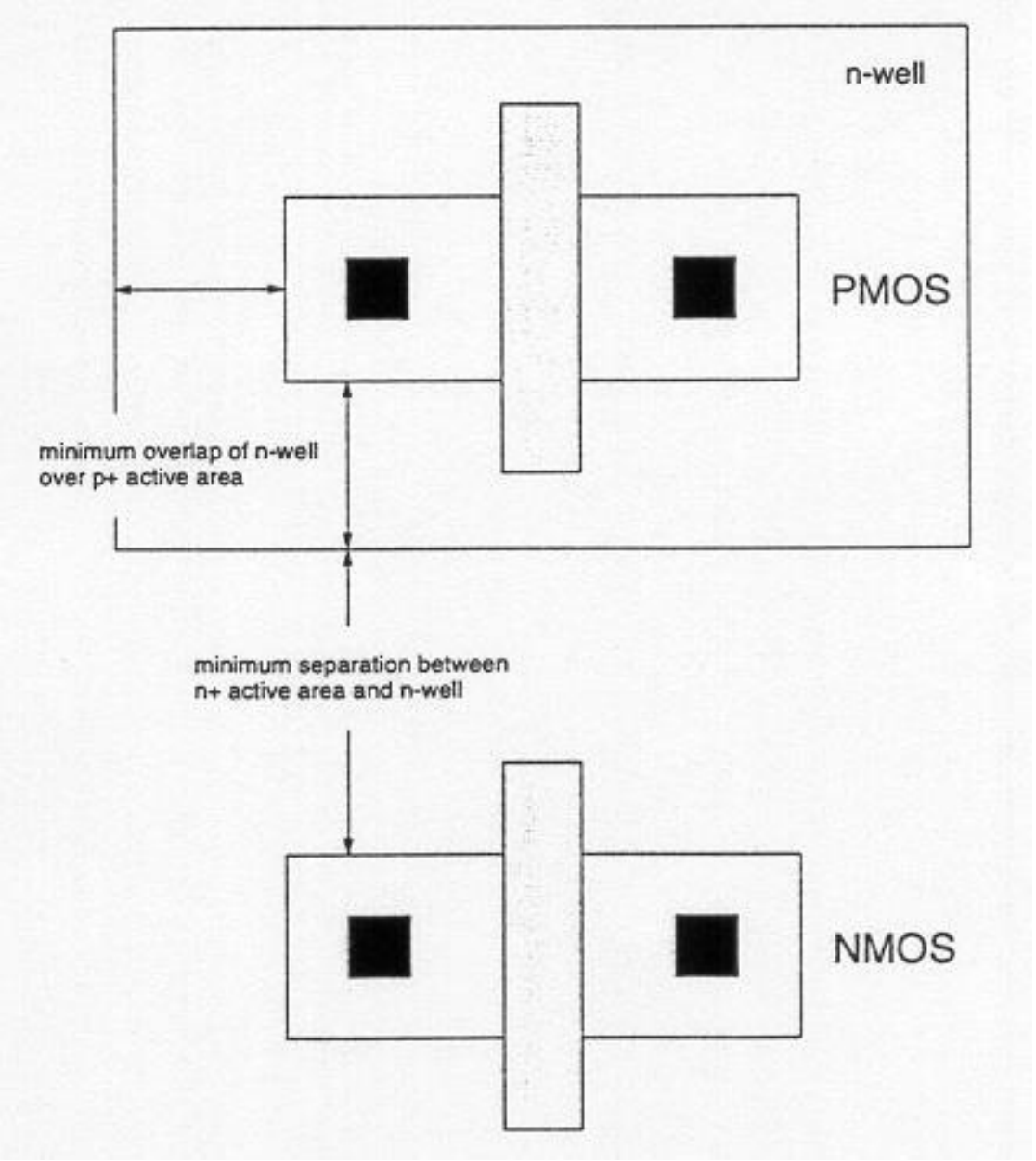
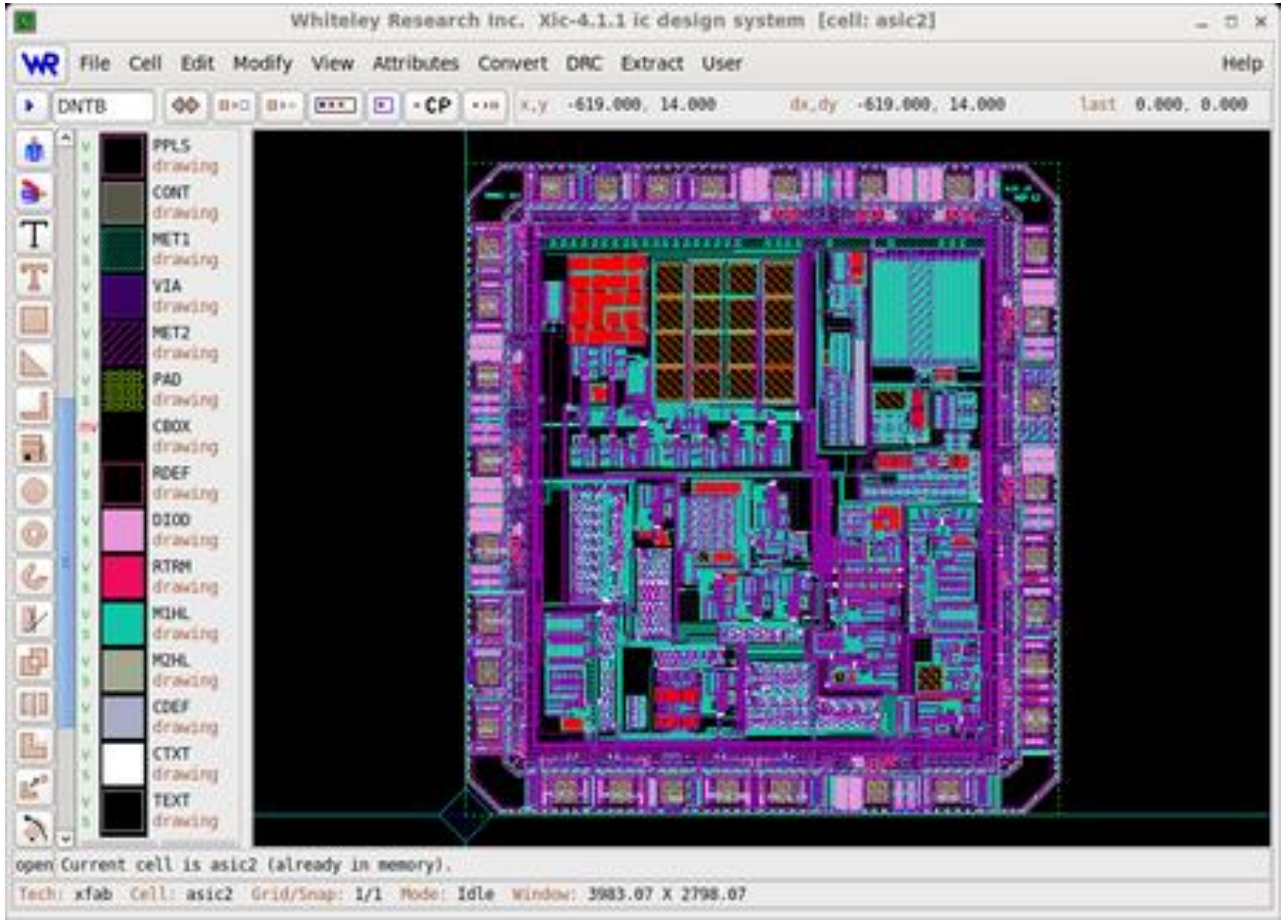


Figura 3.4: Amplasarea unui tranzistor nMOS si a unui tranzistor pMOS

Portile de siliciu policristalin ale tranzistoarelor nMOS si pMOS sunt în mod obisnuit aliniate. Ultimul pas în proiectarea mastilor il reprezinta interconexiunile locle în metal, pentru nodul de iesire si pentru contactele VDD si GND (figura 3.5).

Trebuie remarcat ca pentru o polarizare corespunzatoare, insula n trebuie, de asemenea, sa aiba un contact VDD.



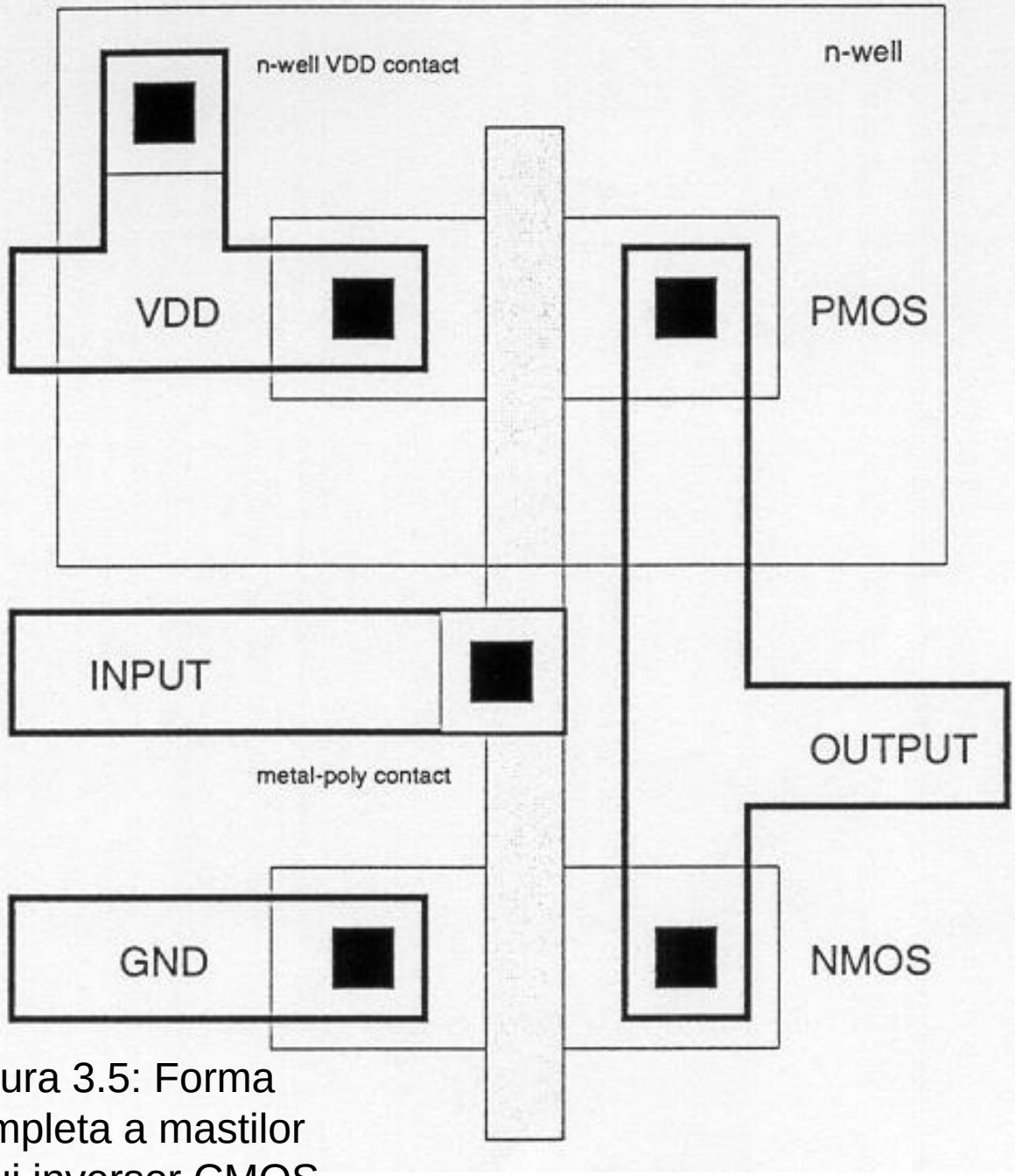
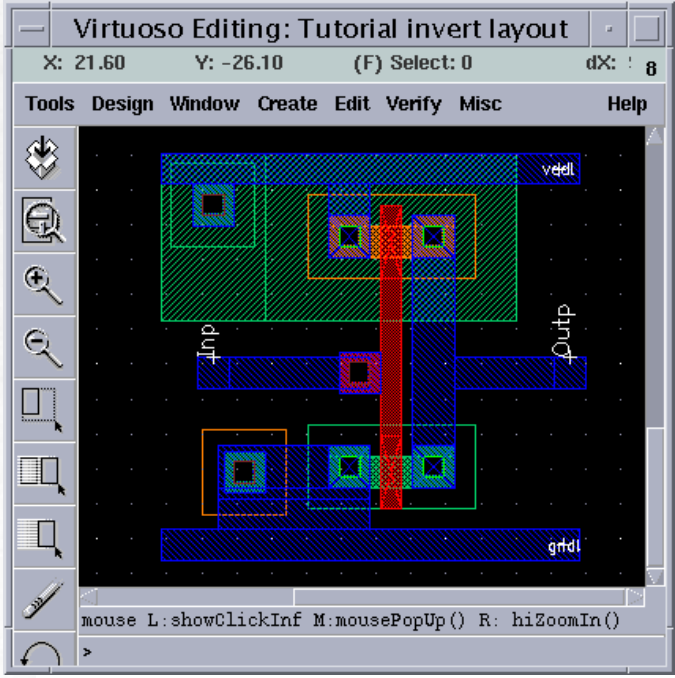
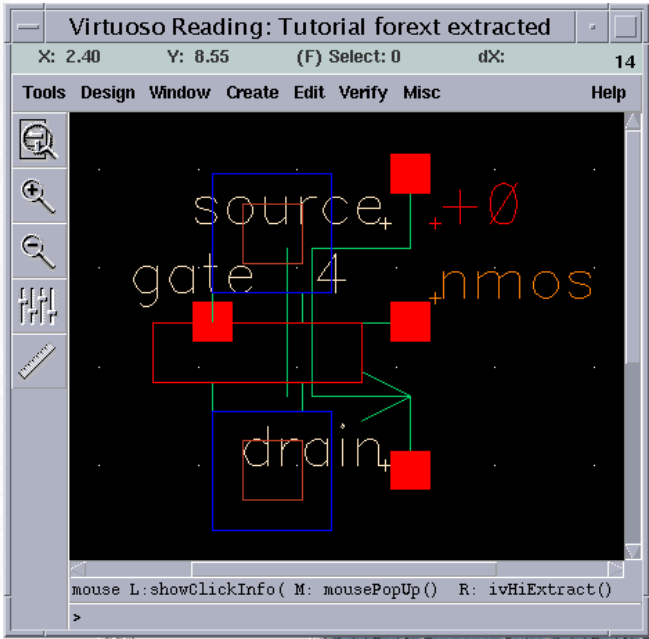


Figura 3.5: Forma completa a mastilor unui inversor CMOS





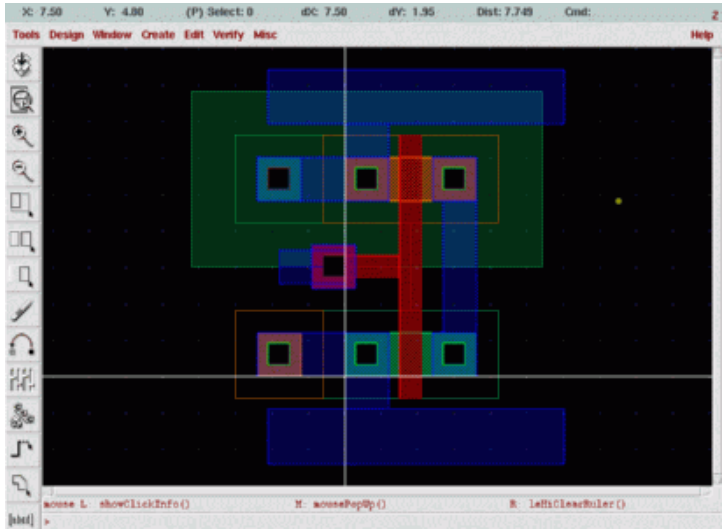
Faza initiala a proiectarii mastilor poate fi simplificata semnificativ prin utilizarea diagramelor de bare sau asa numitor forme simbolice.

În acest caz regulile de proiectare a mastilor sunt pur si simplu abandonate, caracteristicile principale (suprafata activa, liniile de siliciu policristalin, liniile de metal) fiind reprezentate de dreptunghiuri de latime constanta sau simple „bare”.

Scopul diagramelor de bare este acela de a asigura proiectantului o buna întelegere a restrictiilor topologice si de a testa rapid mai multe posibilitati pentru masca optima, fara a desena o diagrama completa a mastii.

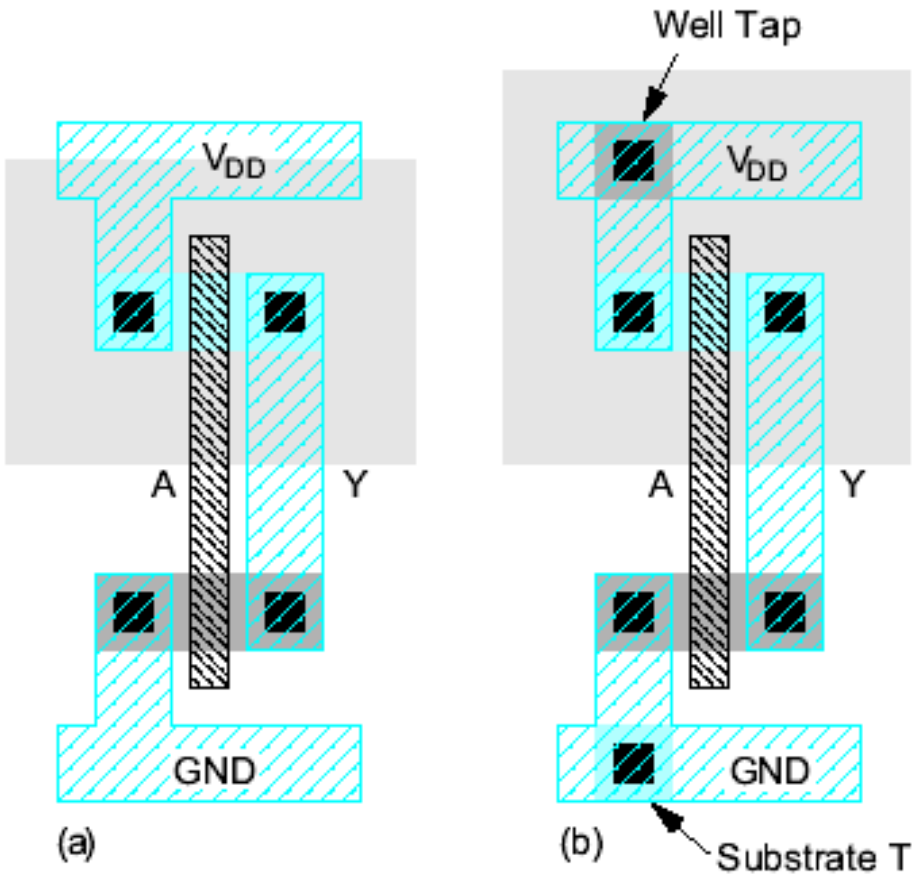
În urmatoarele rânduri, se vor examina mai multe diagrame de bare, care prezinta diferite optiuni pentru mastile unui circuit inversor CMOS.

Final Layout



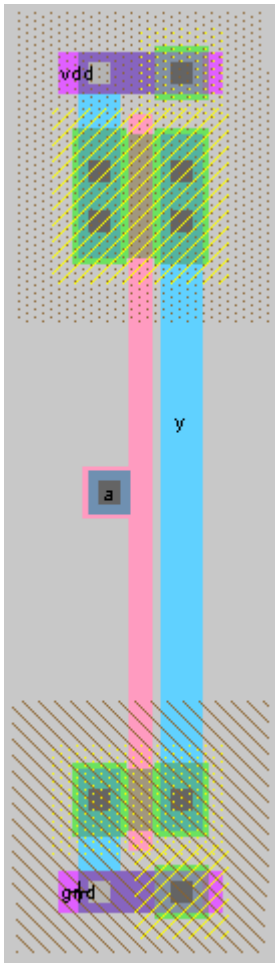
CMOS Inverter Layout

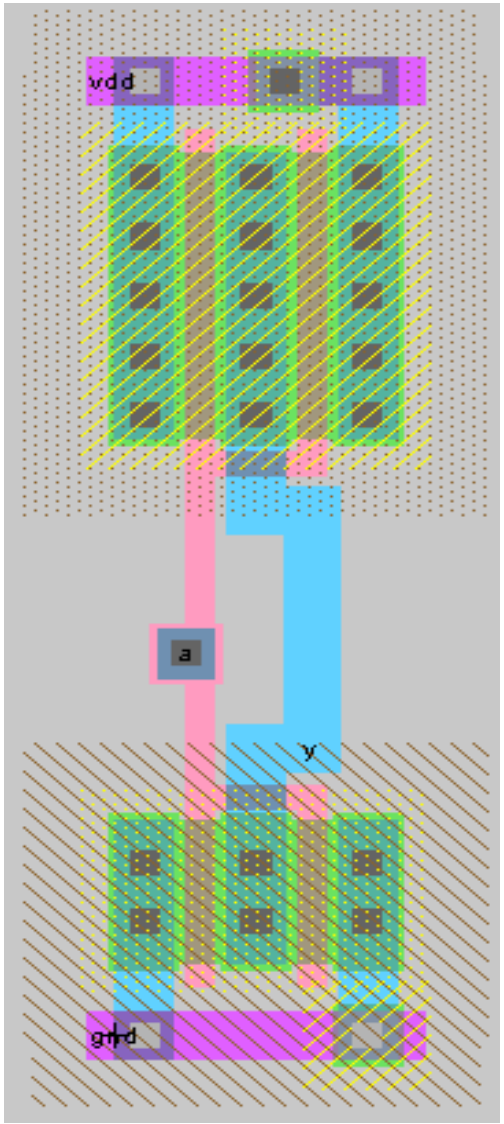
Example: Inverter



Layout using Electric

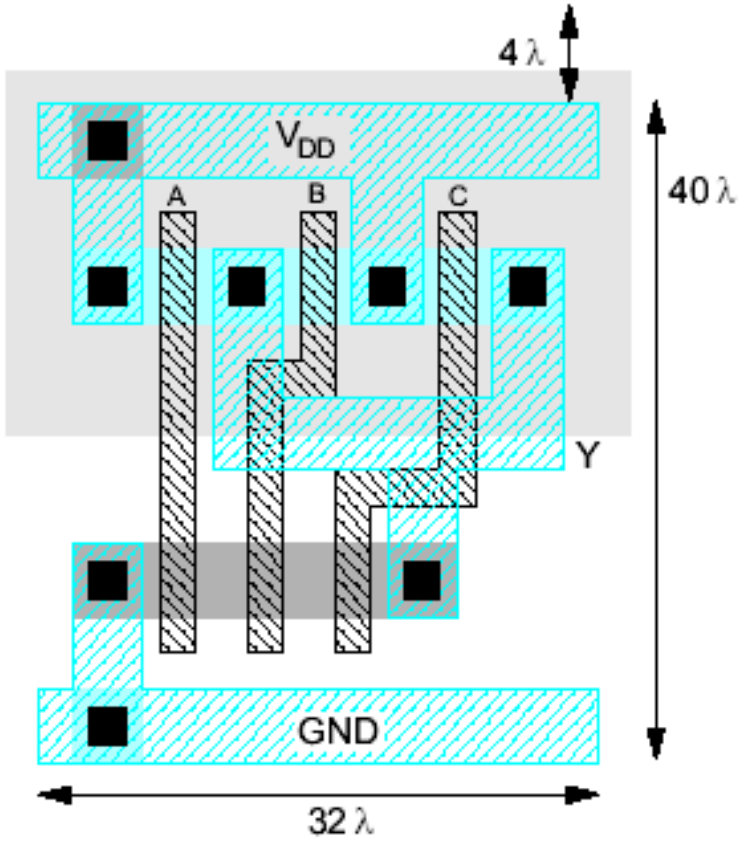
Inverter, contd..

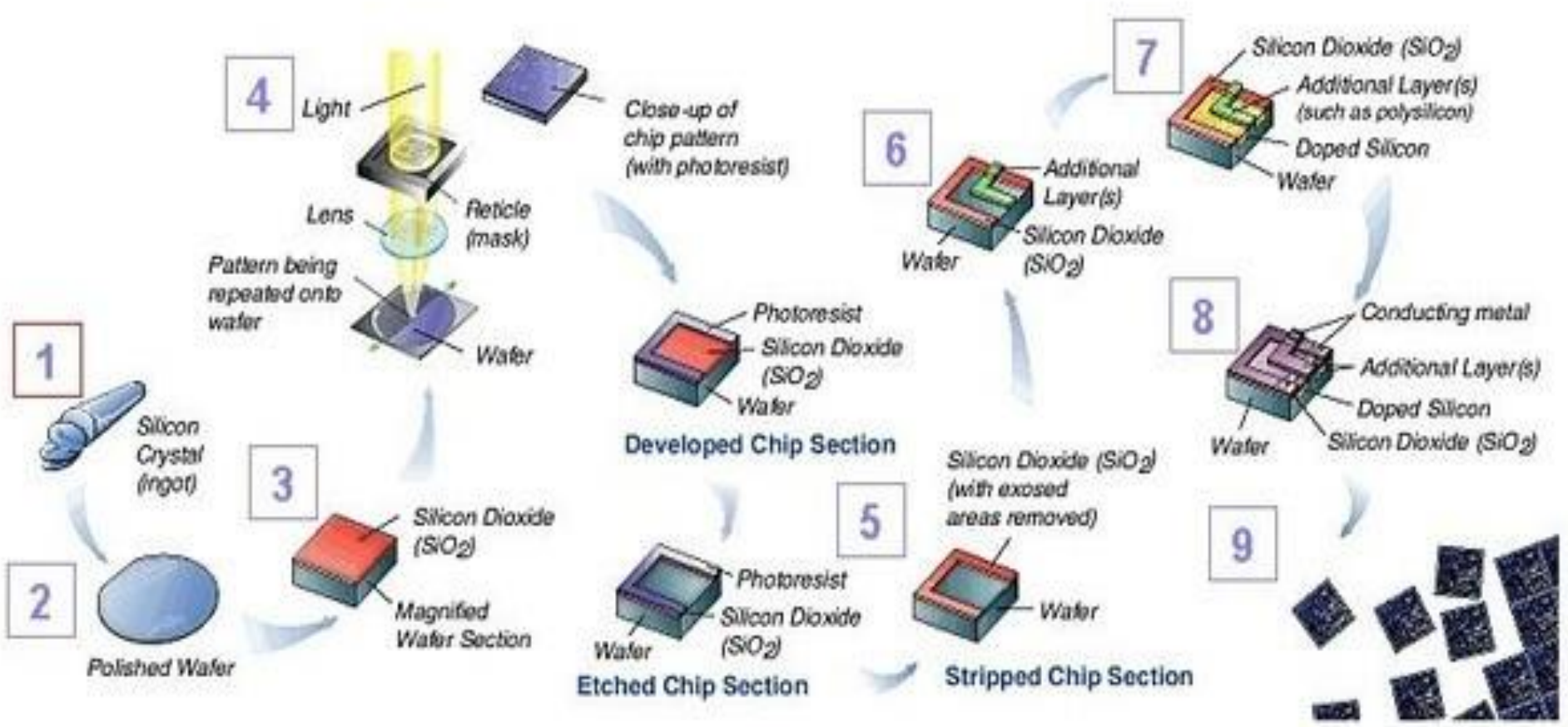




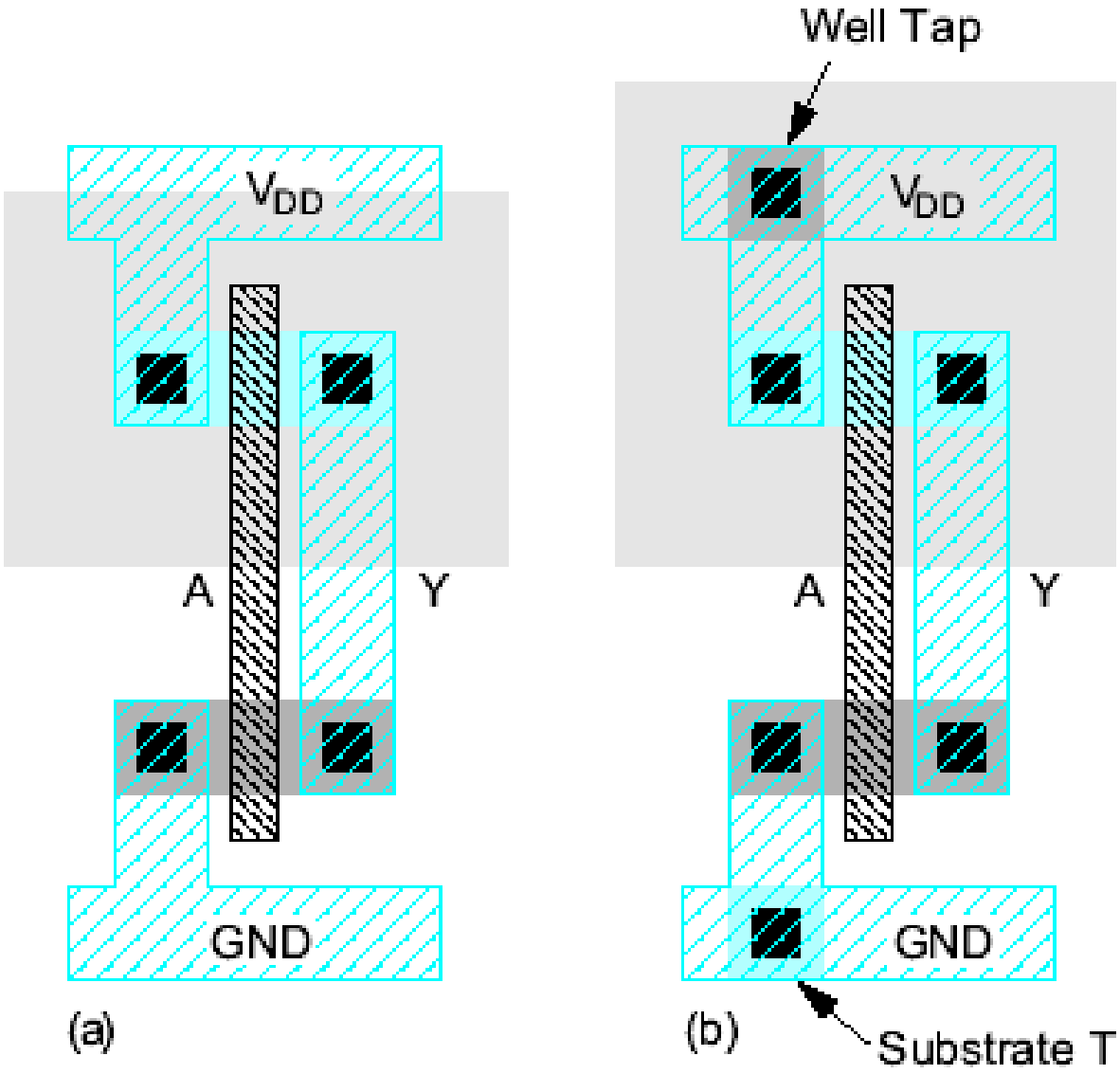
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



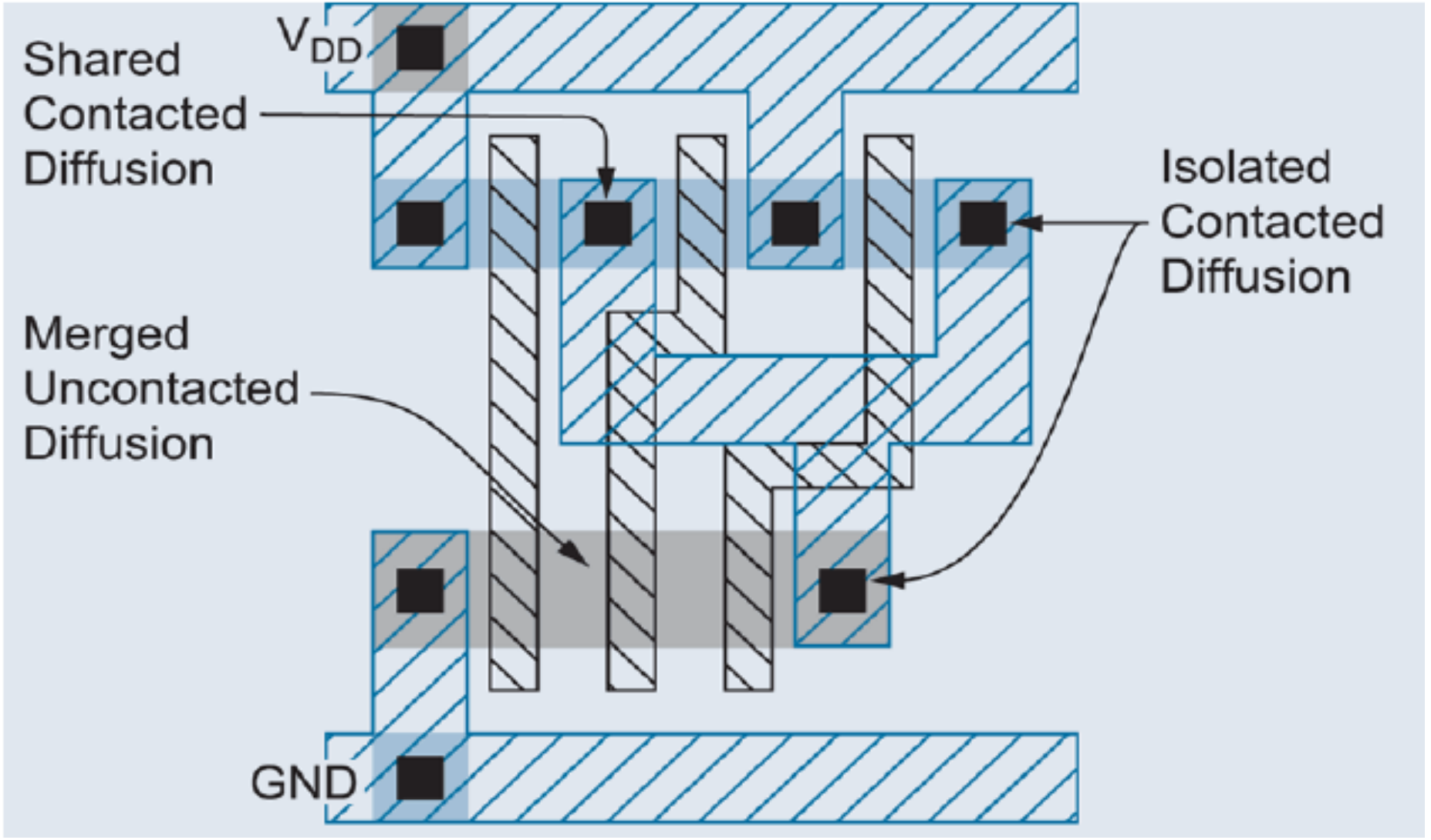

1
Silicon Crystal (ingot)
2
Polished Wafer
3
Silicon Dioxide (SiO_2)
Magnified Wafer Section
4
Light
Lens
Reticle (mask)
Pattern being repeated onto wafer
Wafer
Close-up of chip pattern (with photoresist)
Photoresist
Silicon Dioxide (SiO_2)
Wafer
Developed Chip Section
5
Photoresist
Silicon Dioxide (SiO_2)
Wafer
Etched Chip Section
Silicon Dioxide (SiO_2) (with exposed areas removed)
Wafer
Stripped Chip Section
6
Additional Layer(s)
Silicon Dioxide (SiO_2)
Wafer
7
Silicon Dioxide (SiO_2)
Additional Layer(s) (such as polysilicon)
Doped Silicon
Wafer
8
Conducting metal
Additional Layer(s)
Doped Silicon
Silicon Dioxide (SiO_2)
Wafer
9

Example: Inverter



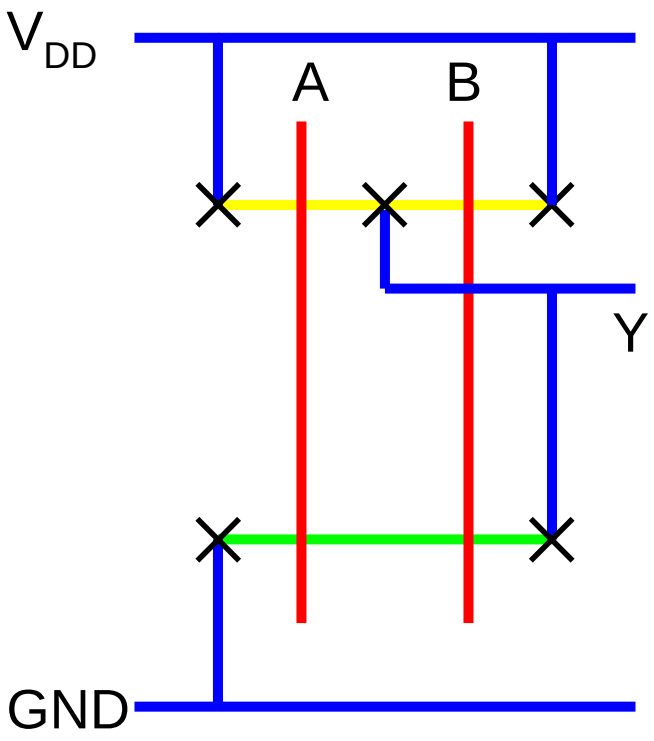
In a good layout, diffusion nodes are shared wherever possible to reduce the diffusion capacitance

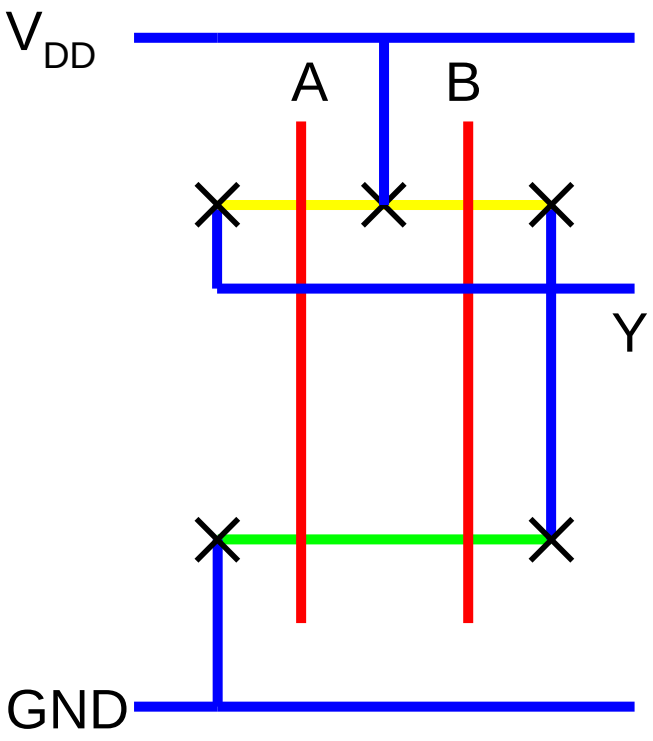
The uncontacted diffusion nodes between series transistors are smaller than the contacted diffusion nodes.



Layout Comparison

- Which layout is better?

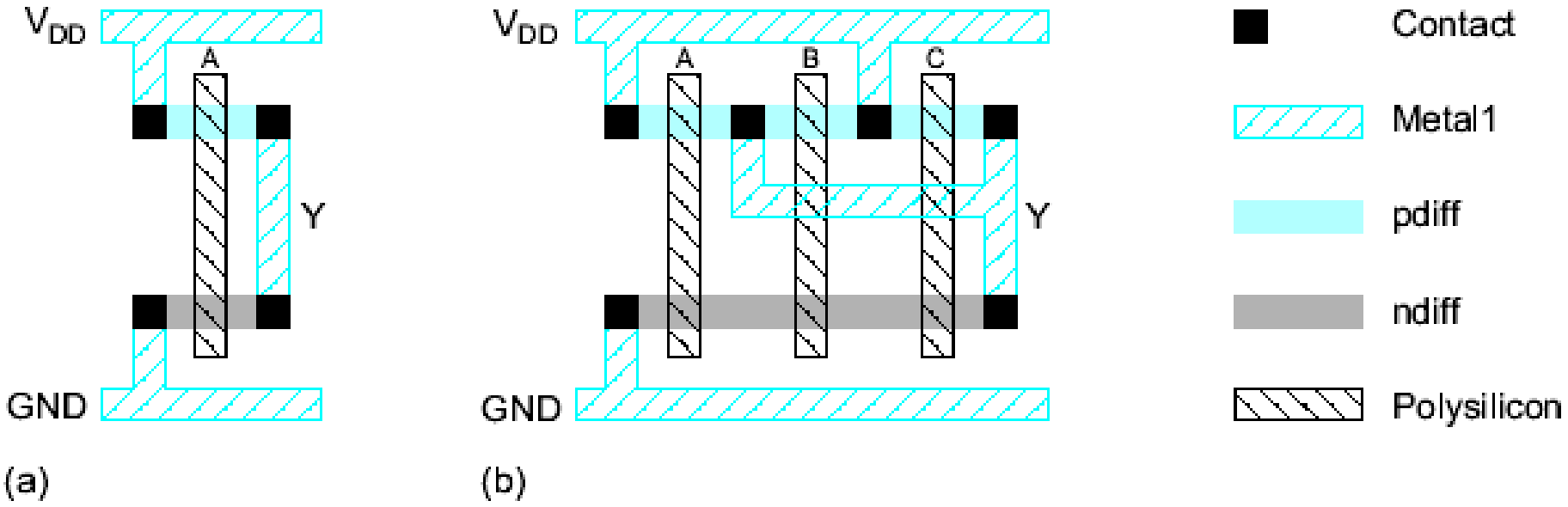




Stick Diagrams

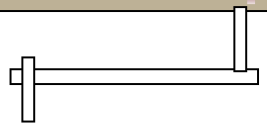
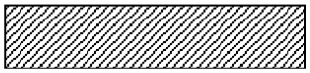
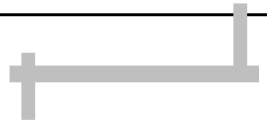
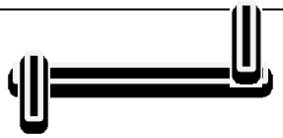
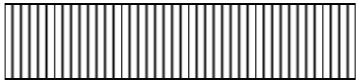
Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers



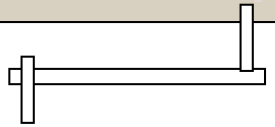
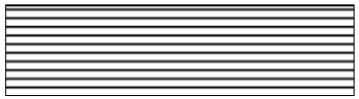
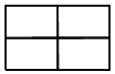
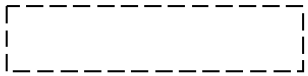
Stick Diagrams

Encoding for nMOS process

Stick Encoding	Layer	Mask Layout Encoding
	Thinox	
	Polysilicon	
	Metal1	
	Contact cut	
NOT applicable	Overglass	
	Implant	
	Buried contact	

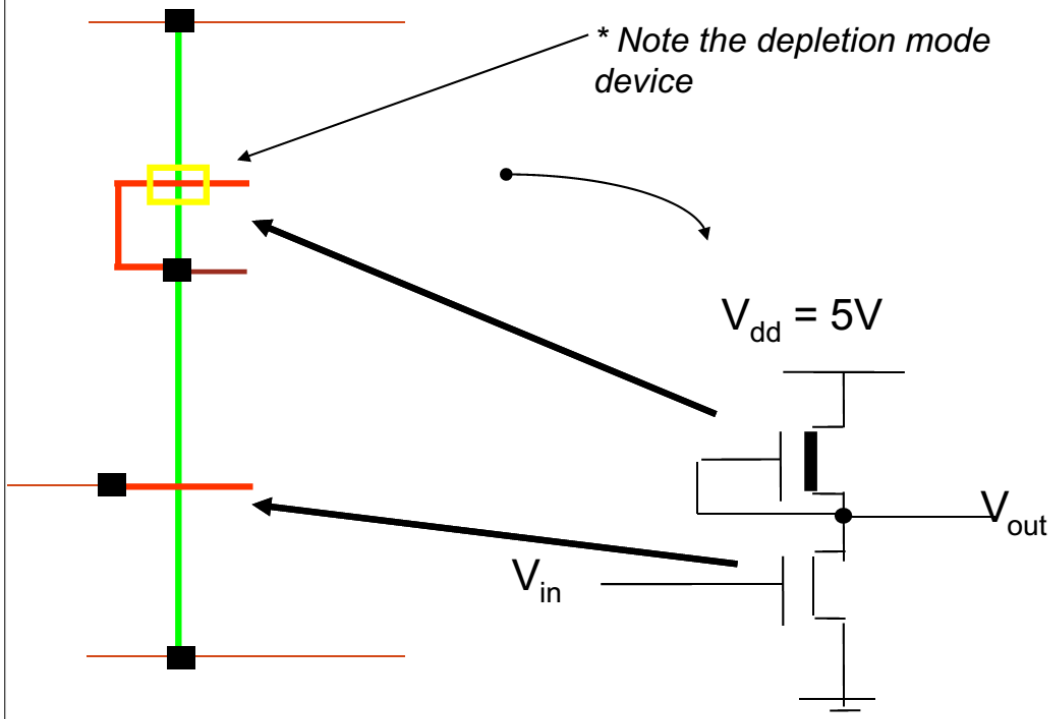
Stick Diagrams

Encoding for pMOS process

Stick Encoding	Layer	Mask Layout Encoding
	P-Diffusion	
Not Shown in Stick Diagram	P+ Mask	
	Metl2	
	VIA	
Demarcation Line	P-Well	
	Vdd or GND CONTACT	

Stick Diagrams

For reference : an nMOS Inverter coloured stick diagram



STICK DIAGRAMS

P- Diffusion

n- Diffusion

Poly silicon

Metal 1

Contact cut

N implant

Demarcation line

Substrate contact

Buried Contact

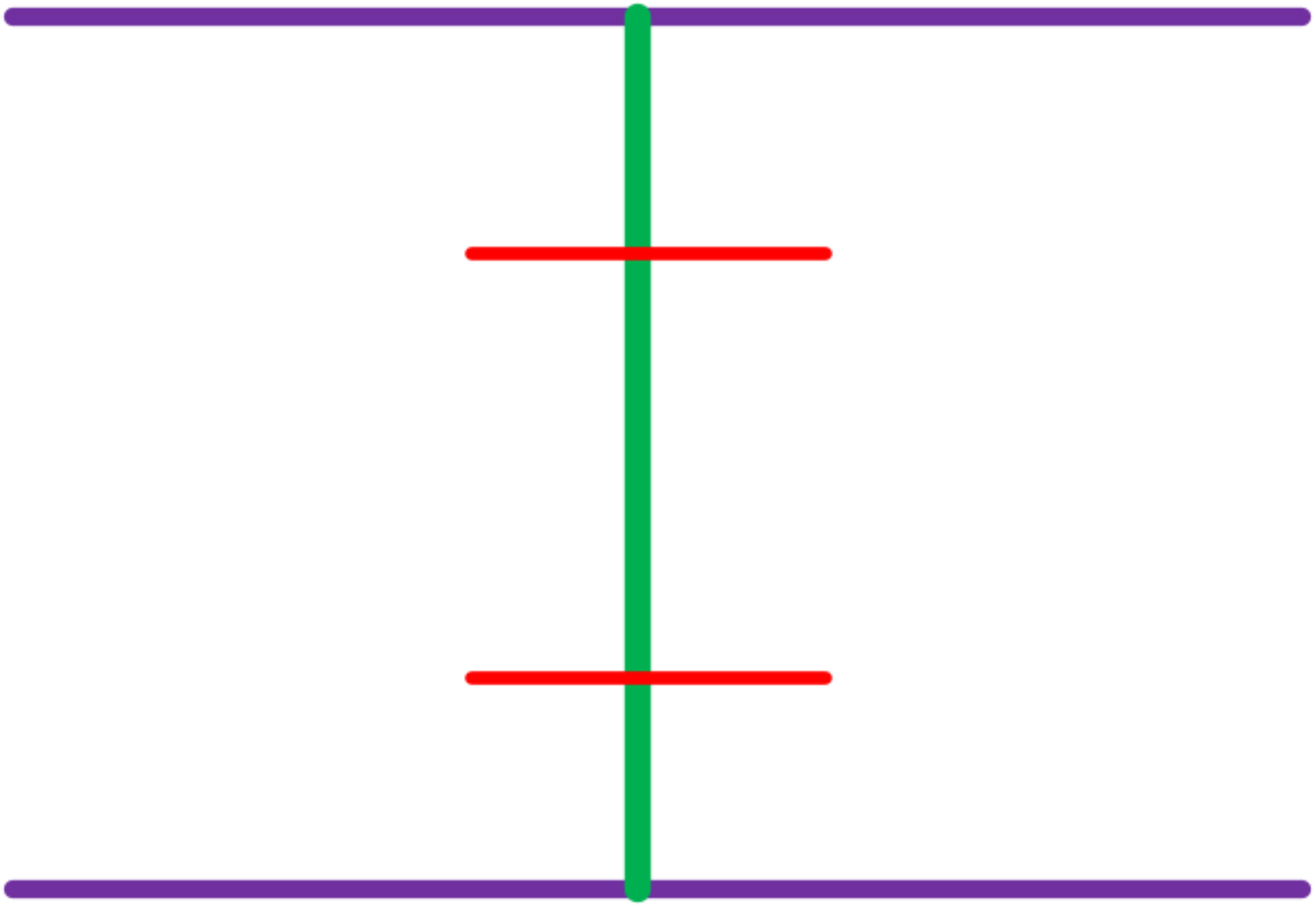
PMOS Enhancement Transistor

NMOS Enhancement Transistor

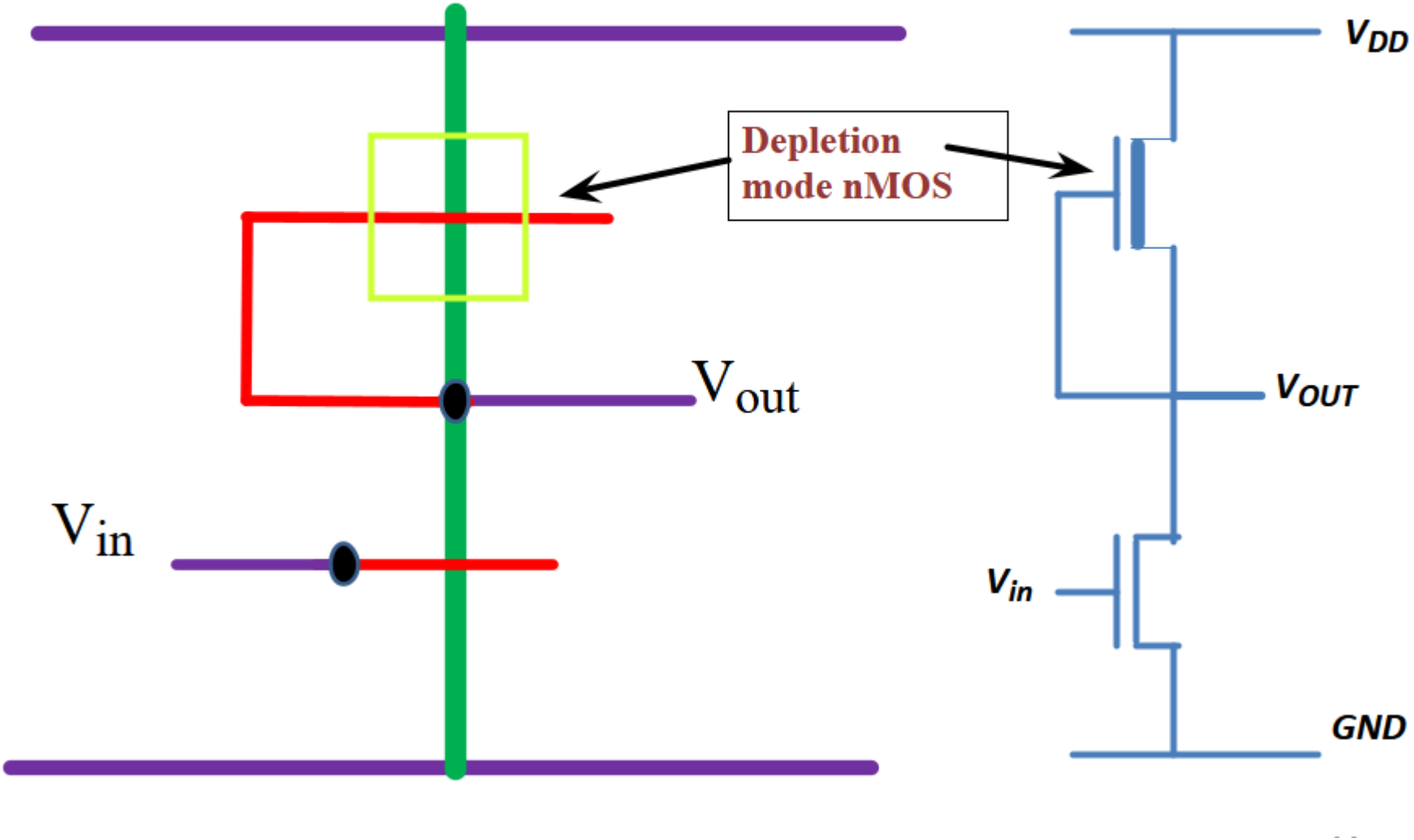
NMOS Depletion transistor

NPN Bipolar Transistor

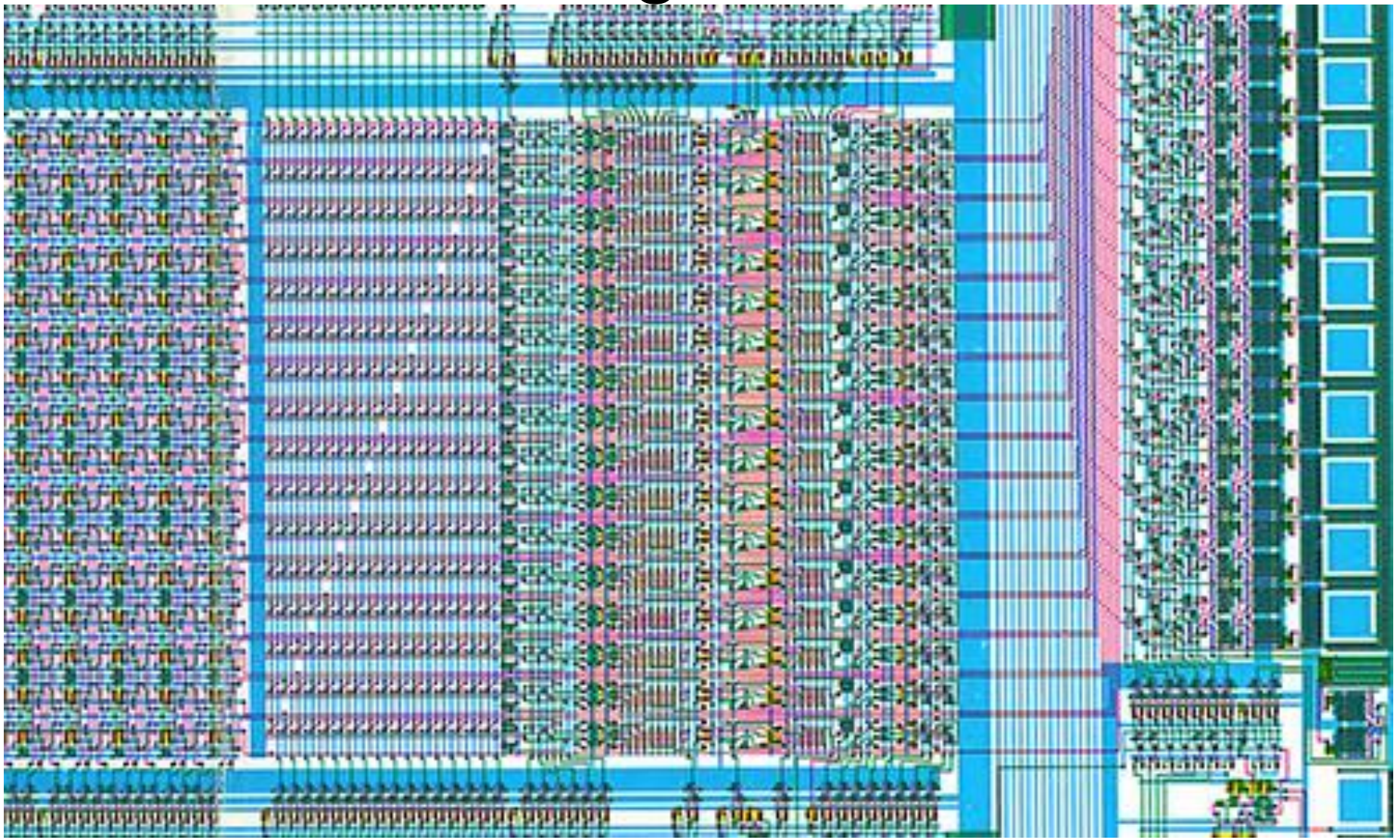
Step 3: Connect poly over thinox wherever transistor required.



Step 4: Connect metal wherever is required and create contact for connection.

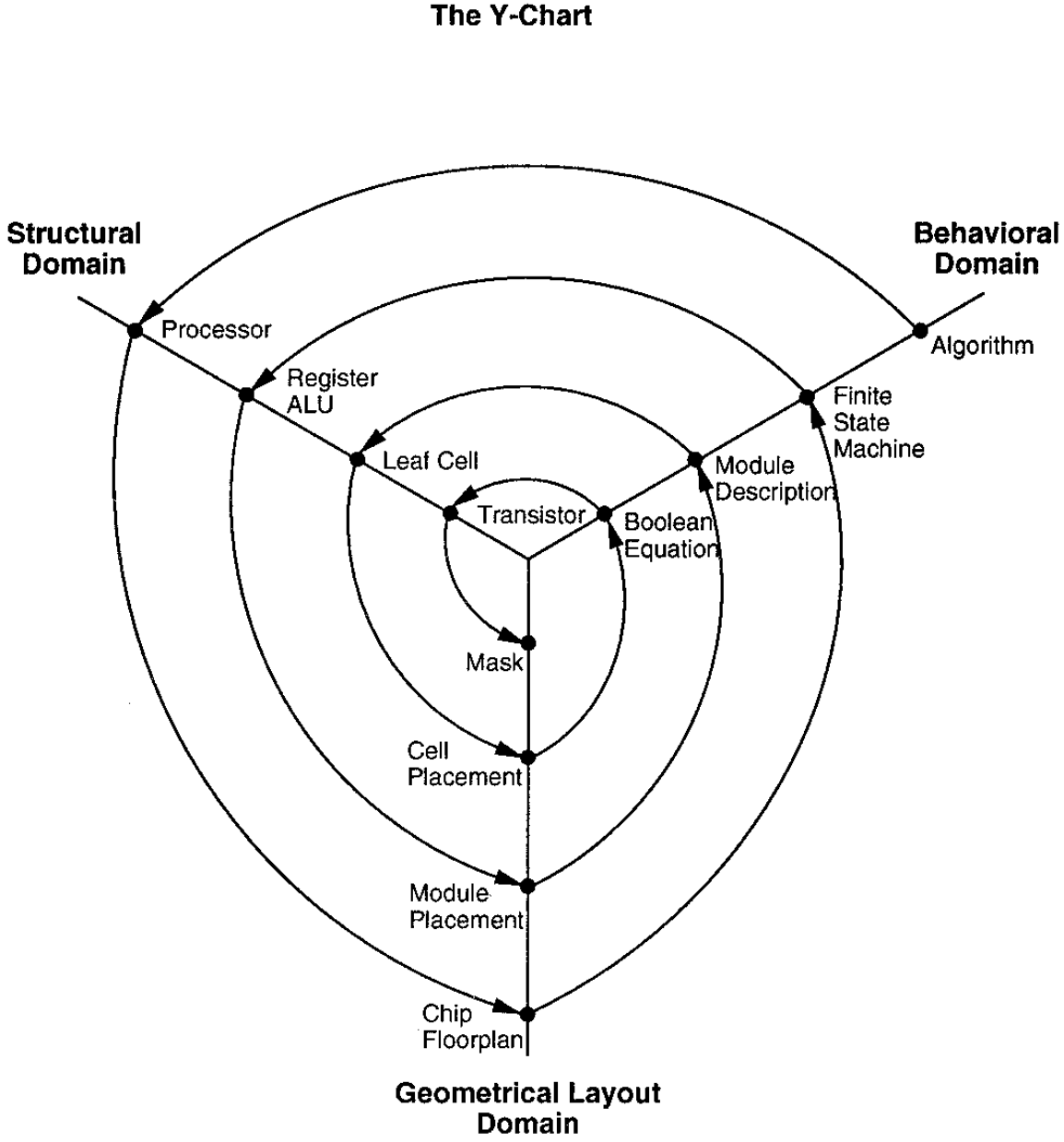


Design VLSI



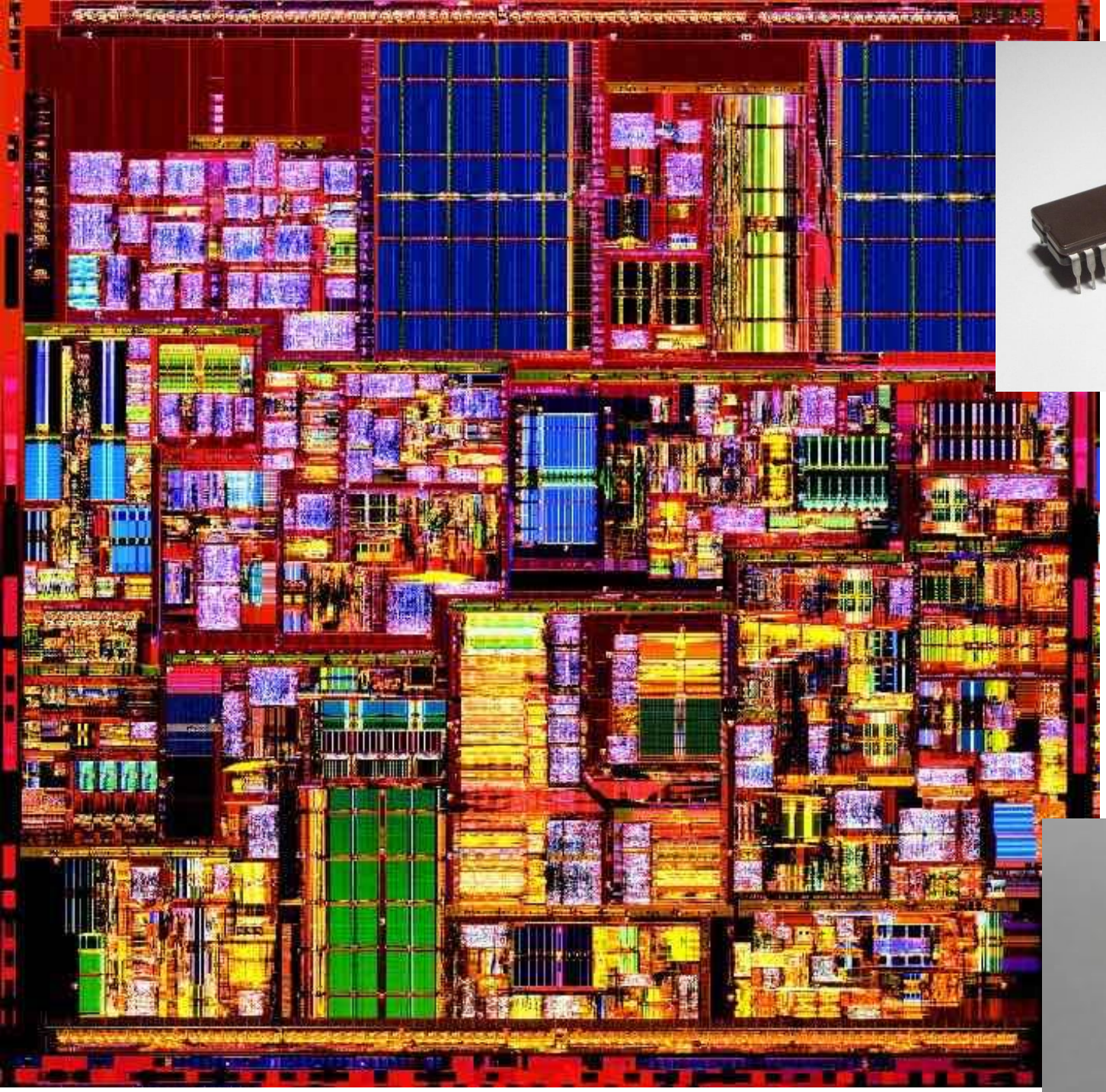
Design VLSI

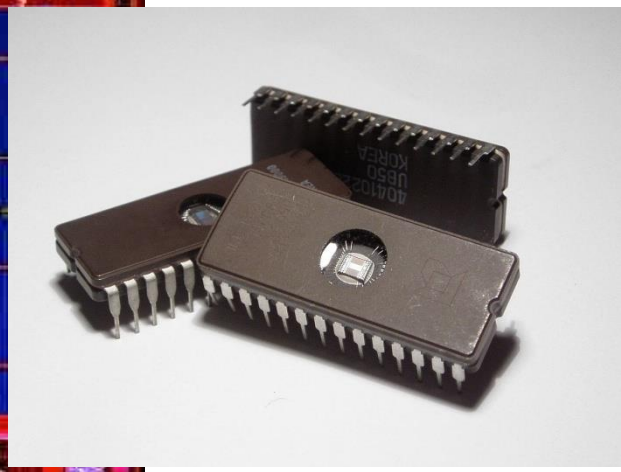
Design VLSI


The Y-Chart
Structural Domain
Behavioral Domain
Processor
Register ALU
Leaf Cell
Transistor
Algorithm
Finite State Machine
Module Description
Boolean Equation
Mask
Cell Placement
Module Placement
Chip Floorplan
Geometrical Layout Domain

Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

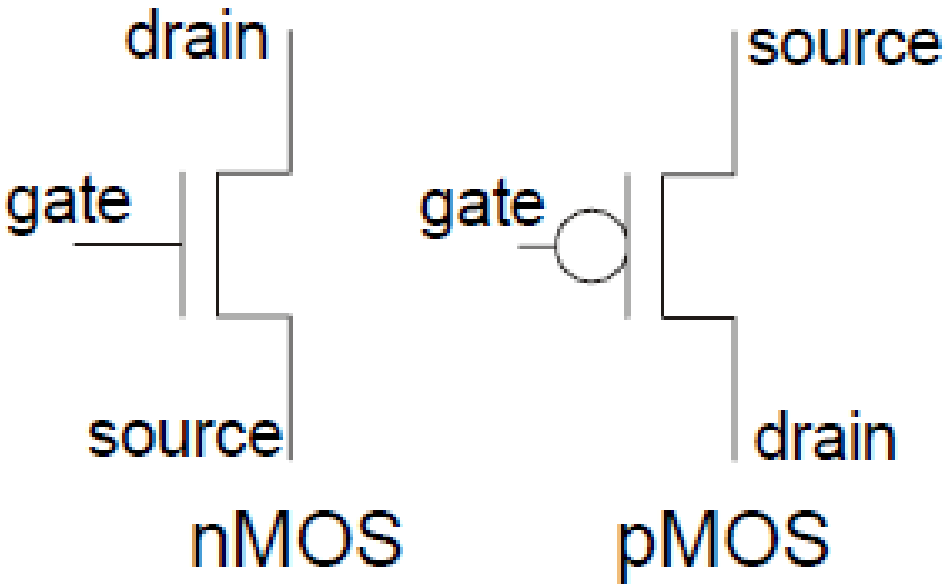


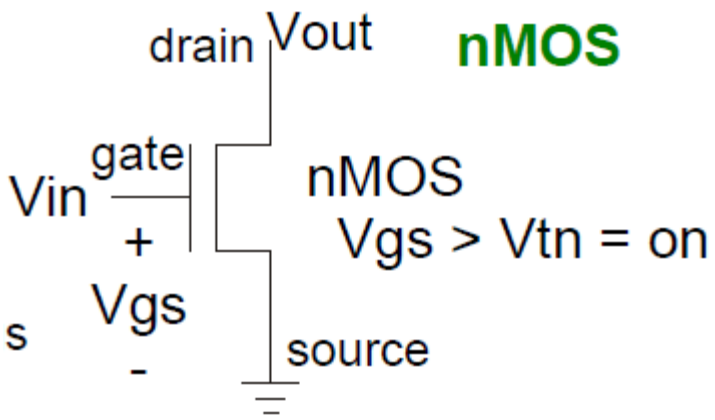


3.5 Porti logice complexe CMOS. Calea Euler

Realizarea unor functii booleene complexe (care pot include mai multe variabile de intrare si mai multi termeni de tip produs) în mod obisnuit necesita o retea serie-paralela de tranzistoare nMOS, care constituie asa numita retea trage-jos (pull-down), si o retea corespondenta duala de tranzistoare pMOS, care constituie reteaua trage-sus (pull-up).

Figura 3.10 prezinta diagrama de circuit si graful corespunzator ale retelei unei porti logice complexe CMOS. Odata ce topologia retelei nMOS (trage-jos) este cunoscuta, reteaua trage-sus poate fi usor construita folosind conceptul de graf dual.



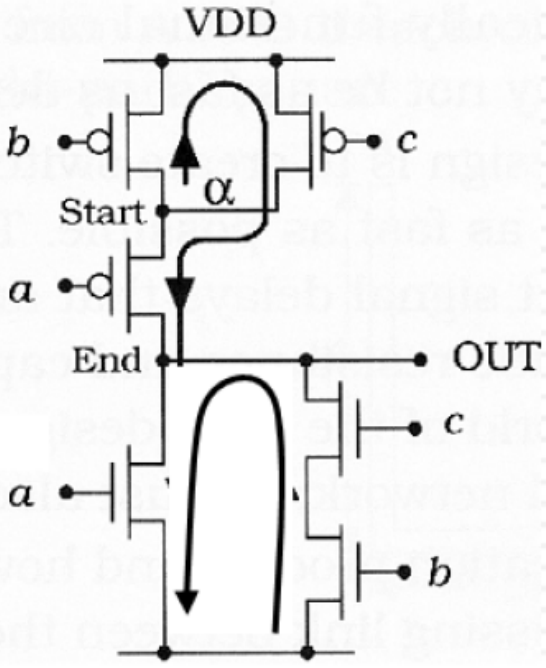


Euler "Path"

- Euler "Path"
  - simplified layout methodology for multi-input circuits; based on Euler Graphs
  - see textbook for full Euler Graph method; unnecessarily confusing for most students
  - used to determine what order (left to right) to layout transistors
  - identifies if all transistors will fit onto a single (non-broken) active strip
- Method
  - try to draw a loop through all transistors
  - separate loop for nMOS and pMOS
  - starting point can be anywhere; may need to try different points to achieve goals

Euler "Path" (2)

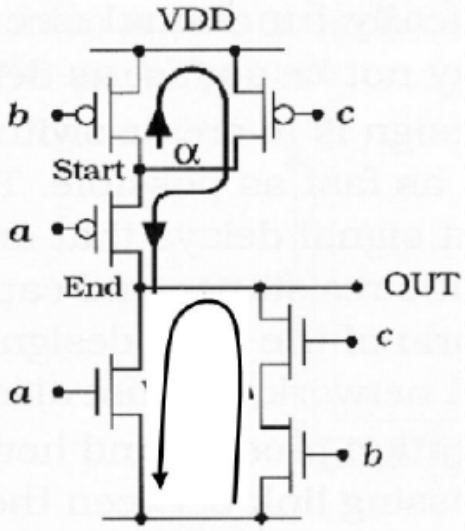
- Rules
  - can only trace through each transistor once
  - otherwise layout won't match schemati
  - can only re-cross any point/node once
  - otherwise multiple activestrips will be required to complete layout
  - must trace through nMOS in the same order as pMOS
- may have to rearrange txs in schematic (without changing function) to achieve rules

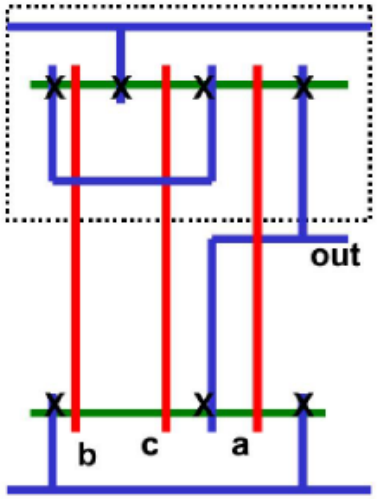


Euler Path Example

$$out = \overline{a + bc}$$

- PMOS Loop
  - start pMOS at nodeα, through 'b'to VDD, through 'c' to α, through 'a'to OUT
  - check loop follows rules
- NMOS Loop
  - trace through same tx order as pMOS
  - start nMOS at ground, through 'b' and to 'c' OUT then through 'a' to OUT again
- Form stick diagram with polys in order b, c, a determined by Euler Path
- Alternative Loops
  - start pMOS loop at OUT, through a, then b, then c.
  - to follow pMOS loop order, start at OUT, through a to ground then b, then c

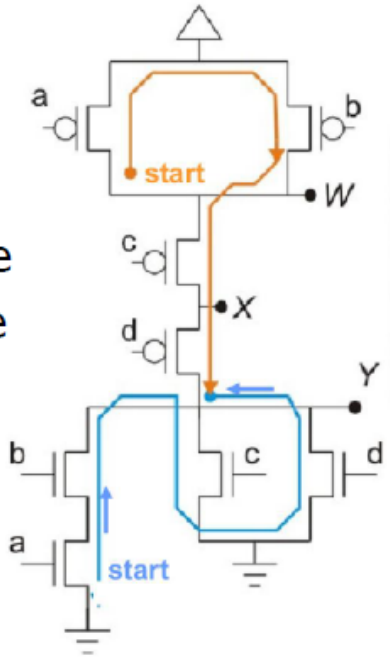


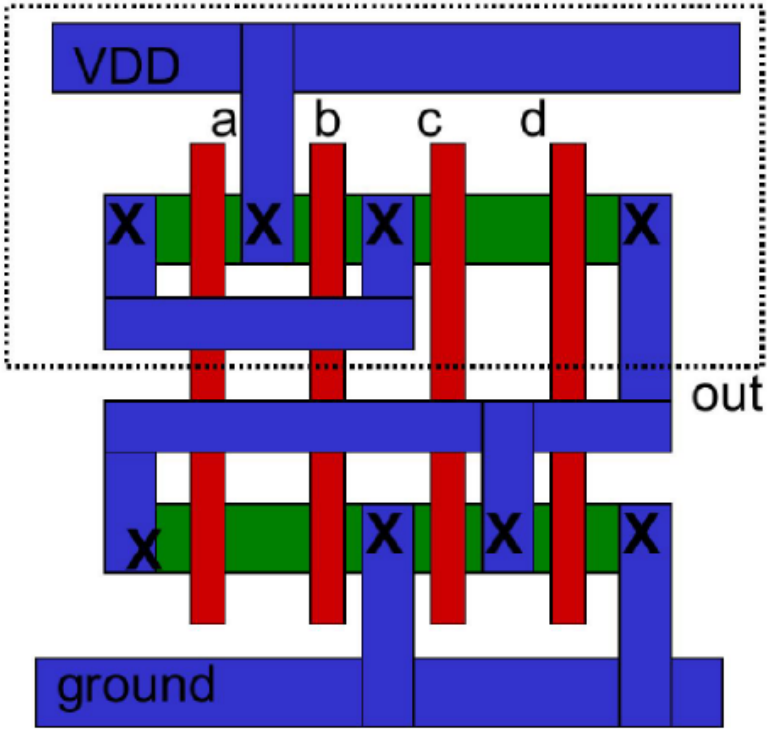


Example

- Circuit with pMOS and nMOS paths

Rule for single active strip: loop can not cross the same point/node more than twice
- pMOS through W twice
- nMOS through Y twice

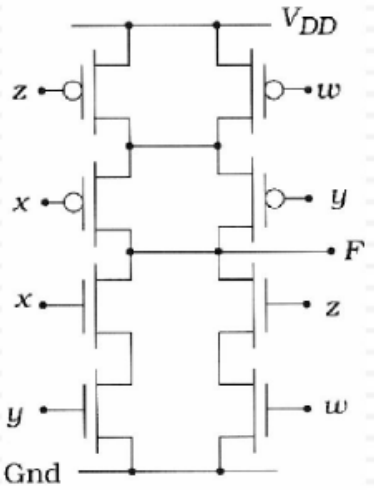




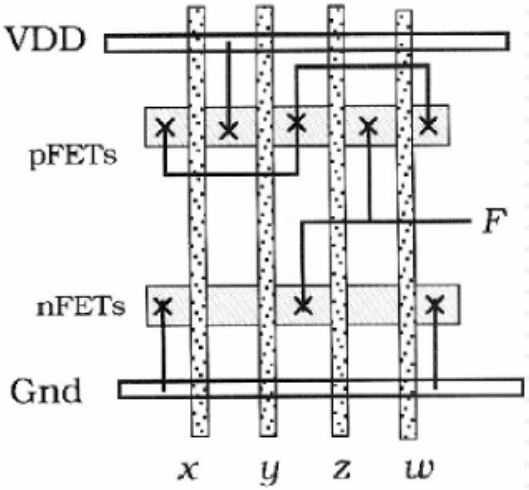
- Shows layout can be constructed with a single p/n active trace
- Order of txs (poly traces) is a,b, c, d, on both p- and n-side

Structured Layout

- General Approach
  - power rails
  - horizontal Active
  - vertical Poly (inputs from top/bottom)
  - Metal1 connects nodes as needed in schematic
- Structured Layout
  - AOI circuit figure
  - useful for many logic functions
  - see examples in textbook
- Disadvantages
  - not optimized for speed
  - large S/D regions = higher capacitance
  - interconnect paths could be shorter
- not optimized for area/size



(a) Circuit



(b) Layout wiring

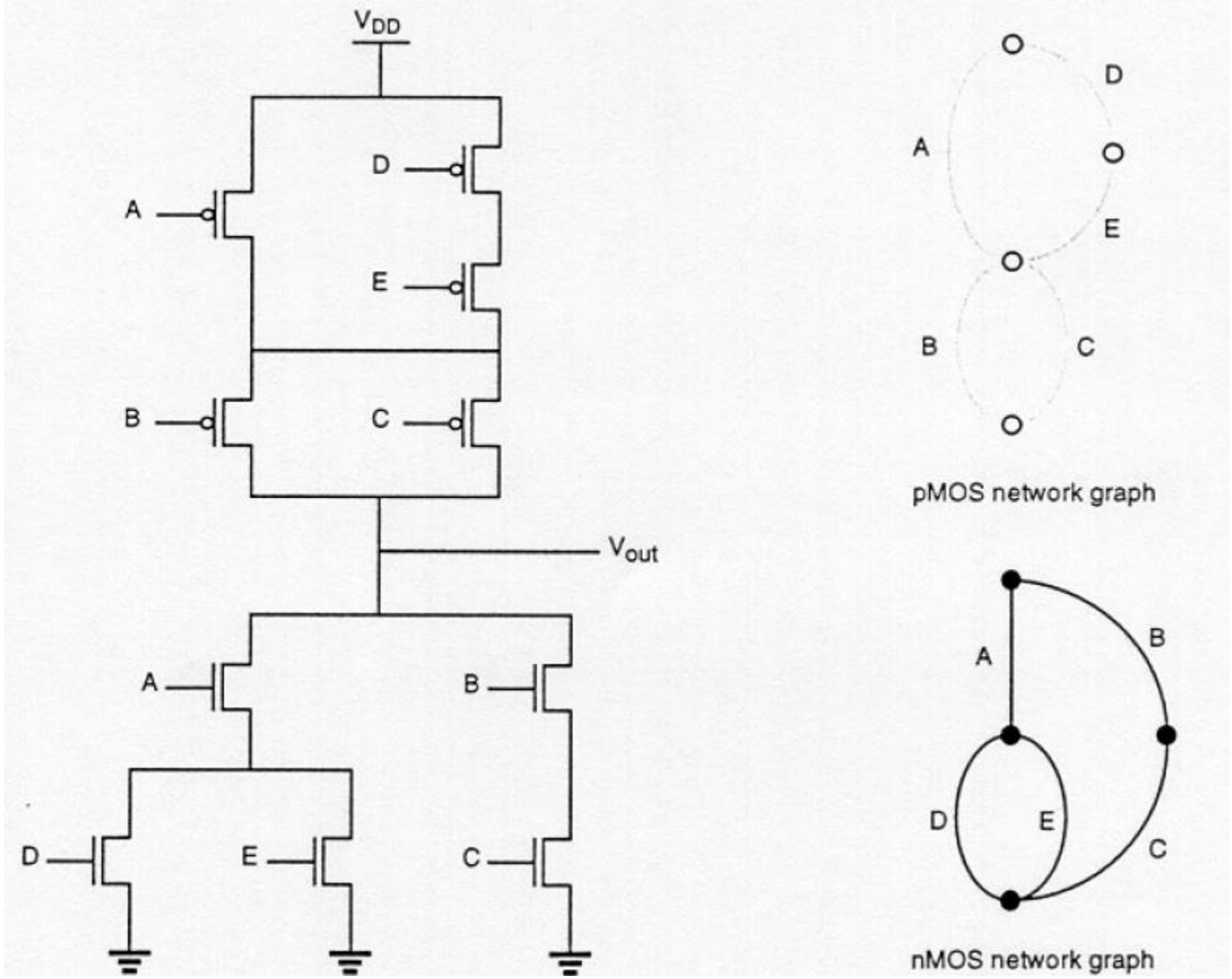
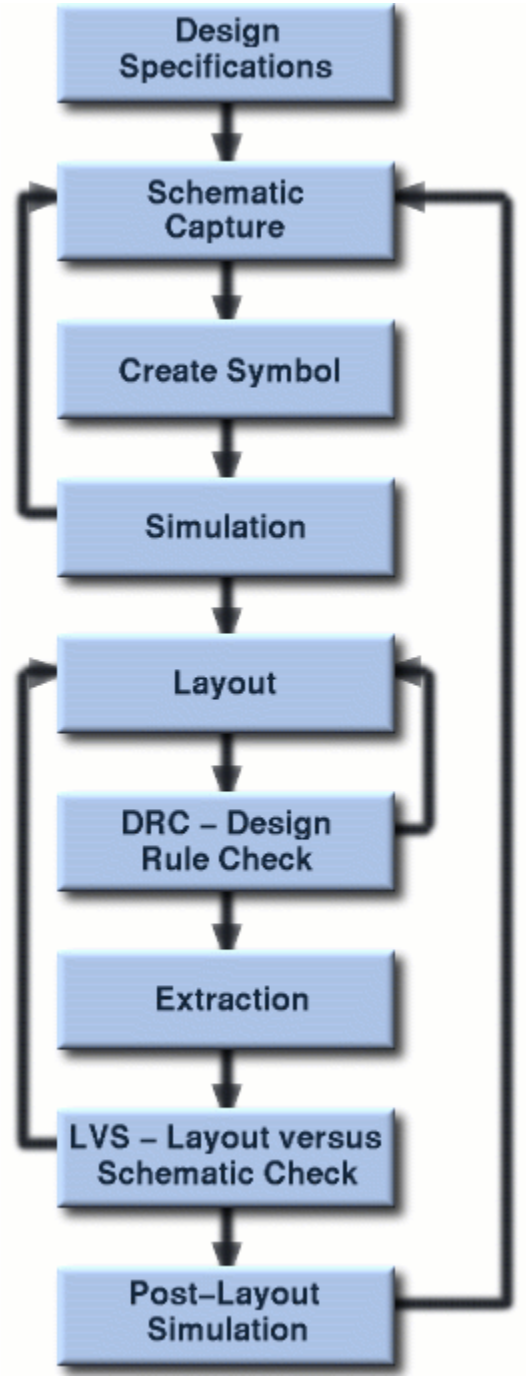
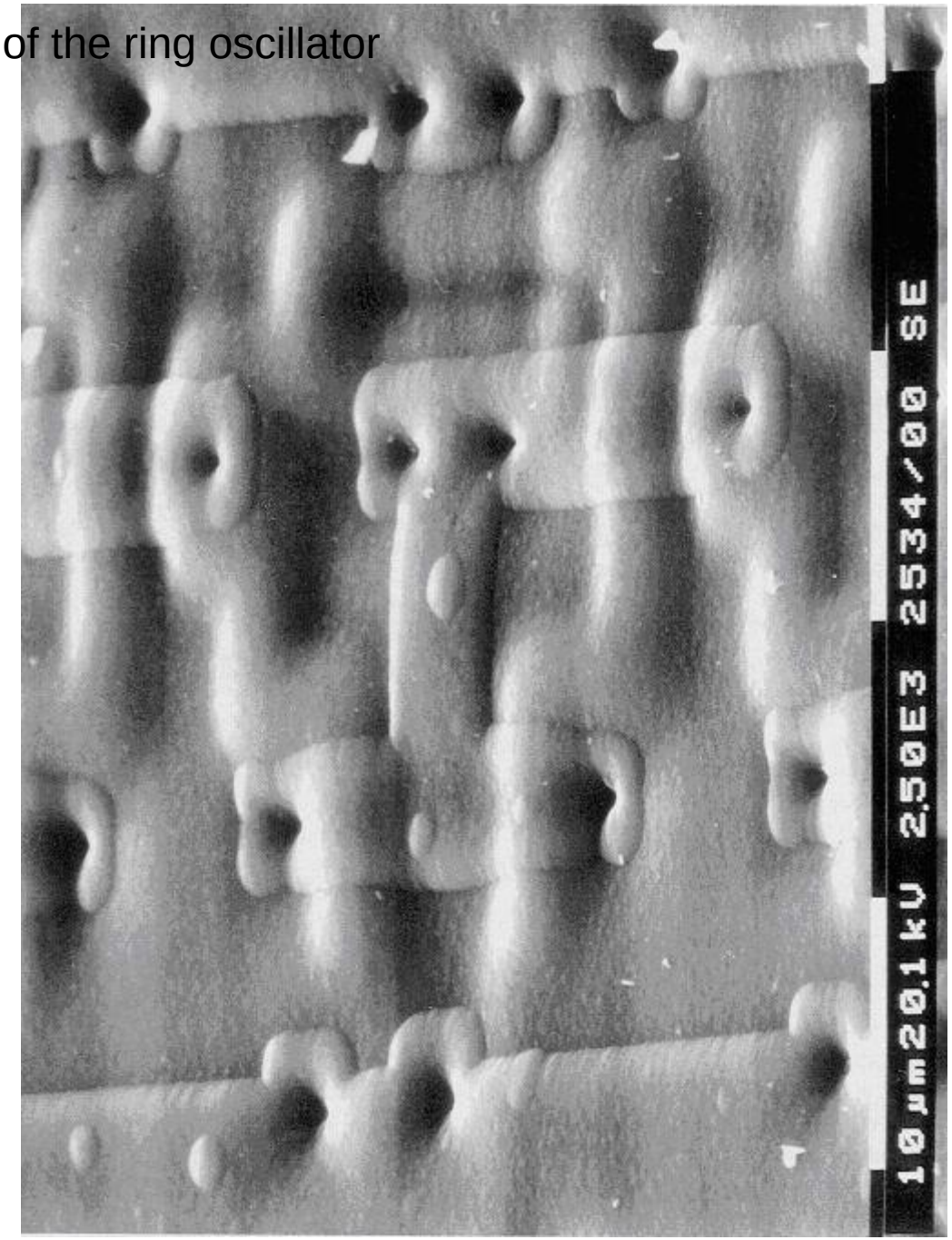
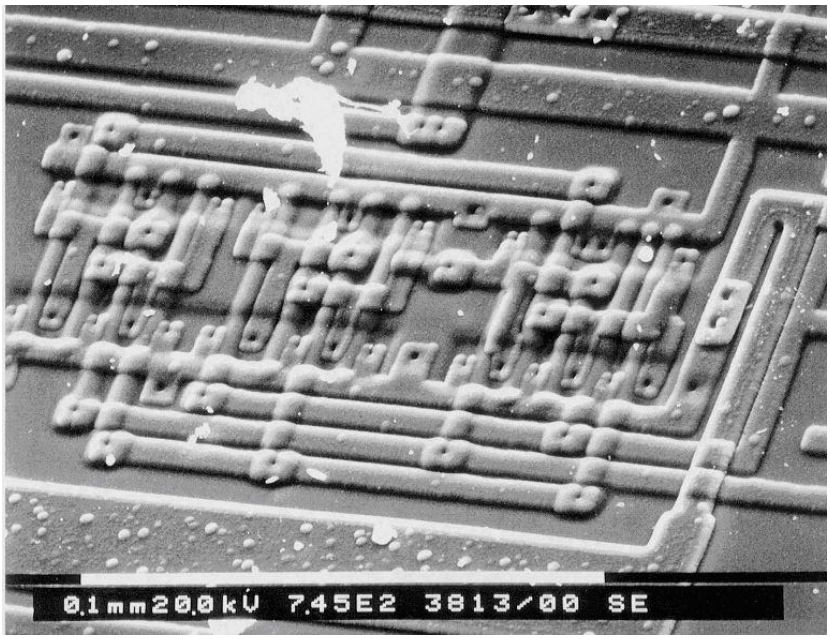


Figura 3.10: O poarta logica complexa CMOS care realizeaza o functie booleana cu 5 intrari


Design Specifications
Schematic Capture
Create Symbol
Simulation
Layout
DRC – Design Rule Check
Extraction
LVS – Layout versus Schematic Check
Post–Layout Simulation

SEM image of part of the ring oscillator




0.1mm20.0kV 7.45E2 3813/00 SE

CMOS AN2 (2 i/p AND gate) Mask Layout