Tehnici de Proiectare Pentru Structuri VLSI

MN-211

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Departament MIB, 3-429

Consultații

Marti 15-18

orice zi disponibila

Examen

Pînă la 20 Decembrie 2024

Bibliografie

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  - Weste and Harris. *CMOS VLSI Design* *(3rd edition)*
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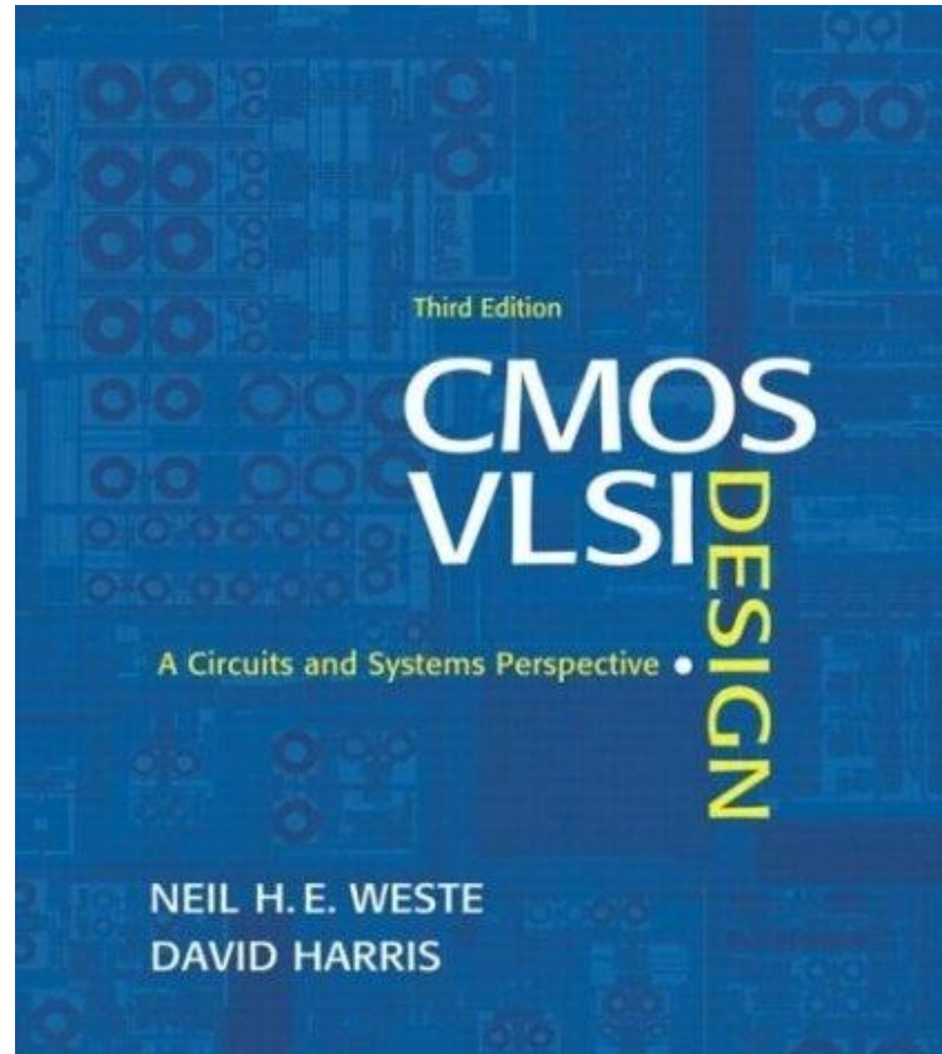


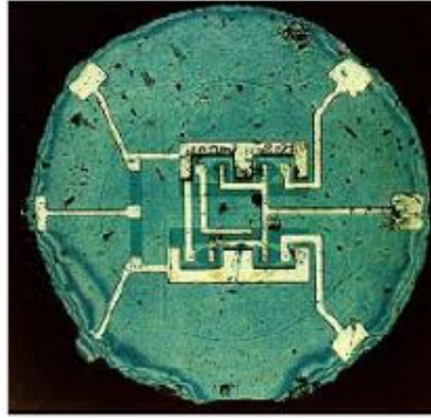
Introduction

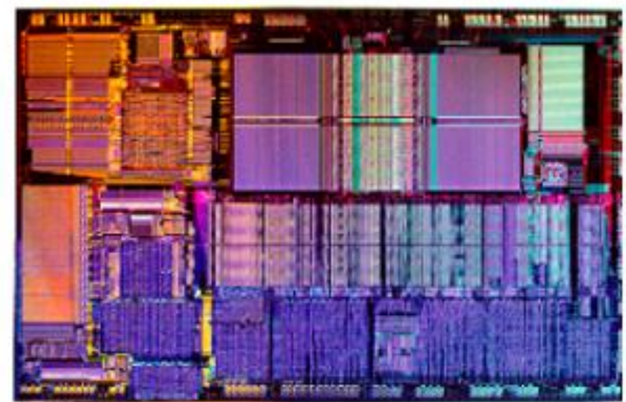
- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- Introduction: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

Capitolul 2.

Tehnologii de fabricatie CMOS si reguli de proiectare

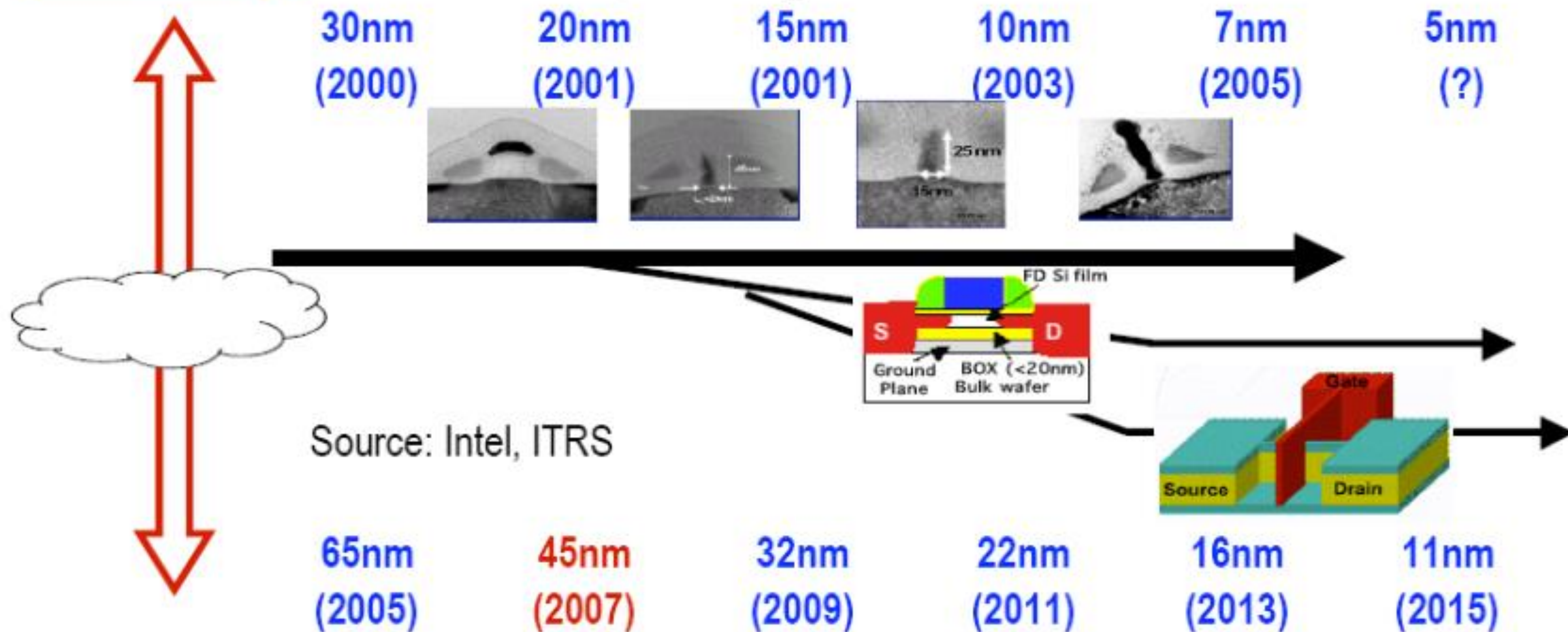
2.1 Introducere
2.2 Procesul de fabricatie – pasii generali (Anexa 1).
2.3 Procesul CMOS cu insula n.
2.4 Tehnologii evoluate de fabricare CMOS.
2.5 Reguli de proiectare.





- 1er transistor en 1947, par Bardeen, Brattain et Shockley ;
  - **Prix Nobel de Physique en 1956 ;**
- 1er Circuit intégré en 1958 par Kilby et Noyce ;
  - **Prix Nobel de Physique en 2000 ;**

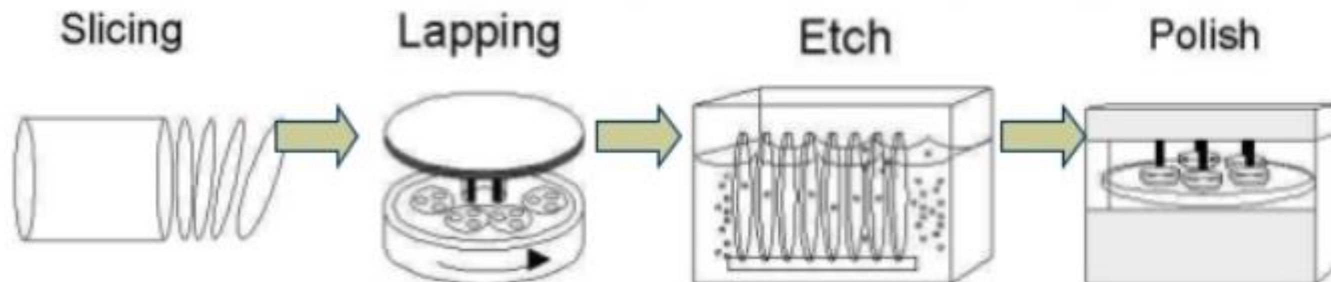
R&D Prototype Technology: Non-classical structures, physics limited, drastic variations, and higher cost



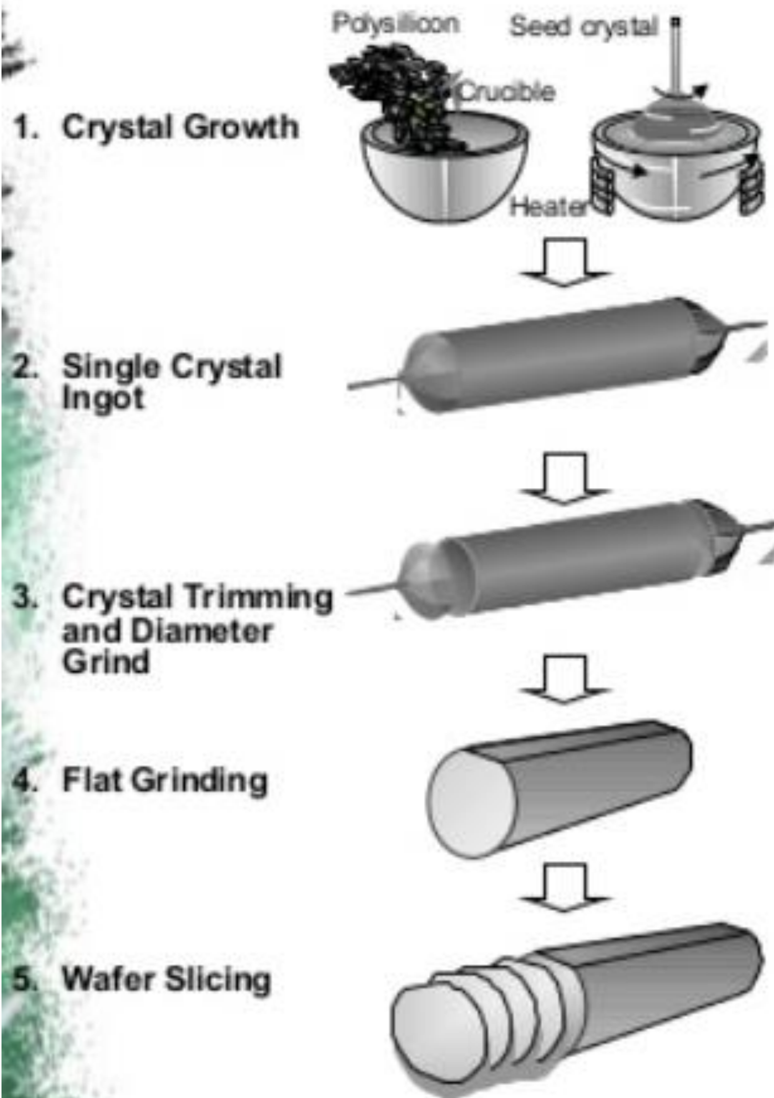
Production Prototypes: Power- and robustness-constrained, adaptive, billion-scale integration, gigaHz operation

CYLINDER OF MONOCRYSTALLINE

- The Silicon Cylinder is Known as an Ingot
- Typical Ingot is About 1 or 2 Meters in Length
- Can be Sliced into Hundreds of Smaller Circular Pieces Called Wafers
- Each Wafer Yields Hundreds or Thousands of Integrated Circuits



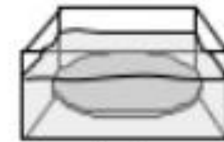
Preparation of Silicon Wafer



6. Edge Rounding

7. Lapping

8. Wafer Etching



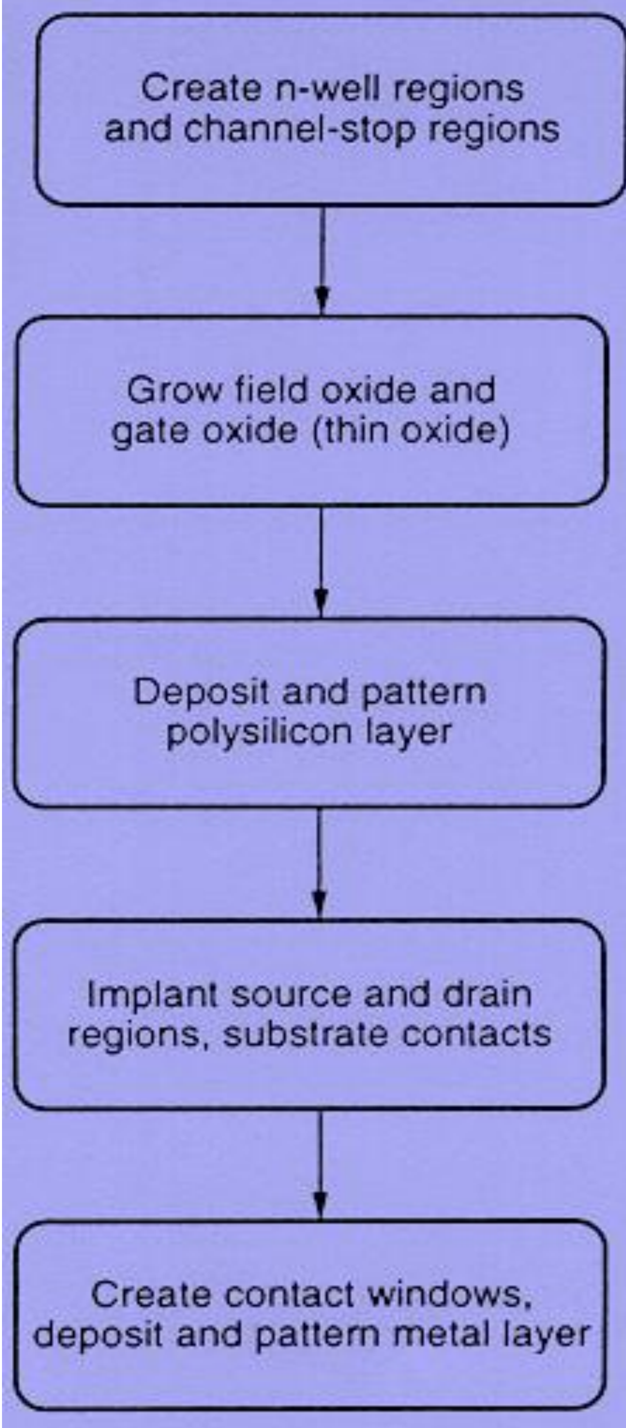
9. Polishing

10. Wafer Inspection

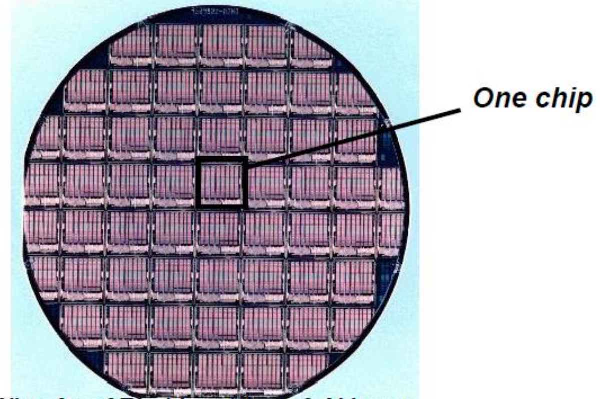
200mm/1990 | 300mm/2001 | 450mm/2012 | 675mm/2019?

(125/150mm - 1981)

9 yrs + 2yrs delay* | 11 yrs + 0yrs delay | 9 yrs + 0yrs delay



CMOS Fabrication



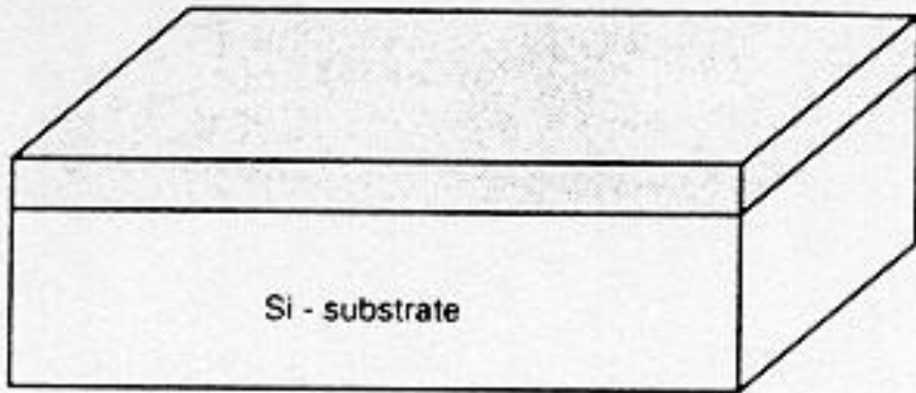
[6" wafer of T0 chips, 1.0μm, 2 Al layers, 1995]

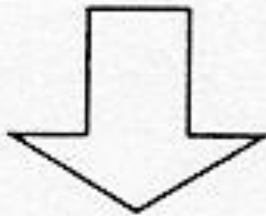
Figura-2.1: Secventa simplificata a procesului de fabricatie a circuitului integrat CMOS n-well (cu insule de tip n) cu un singur strat de polisiliciu, prezentand doar pasii importanti de fabricatie

19.09.2024 a 2-a pereche

Secventa de proces ilustrata in figura 2.1 ar putea parea la prima vedere prea abstracta din cauza faptului ca pasii detaliati de fabricatie nu sunt prezenti. Pentru a intelege mai bine factorii implicati in fabricatia semiconductorilor trebuie detaliati in primul rand unii dintre pasii principali.

Figura-2.2: Pasii de proiectare pentru partitionarea cu dioxid de siliciu.





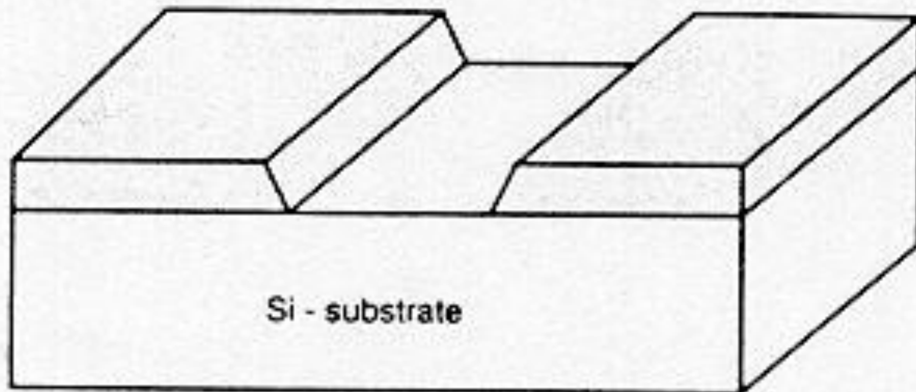
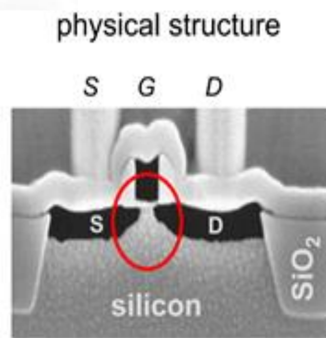
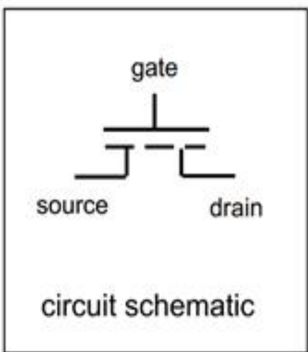
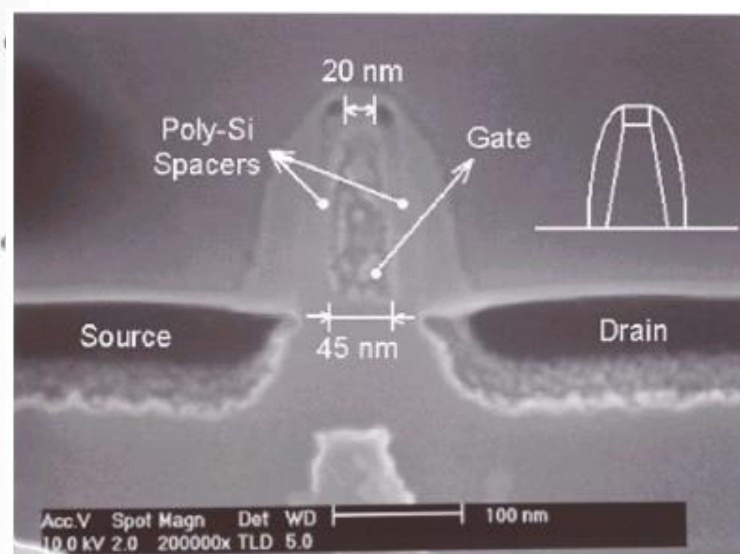


Figura-2.3: Rezultatul unei secvente de transpunere de forme/masti prin litografiere pe dioxid de siliciu, fara a arata pasii intermediari. A se compara structura initiala (sus) si structura pe care a fost transpusa masca(jos) cu figurile 2.2(b) si respectiv 2.2(g).

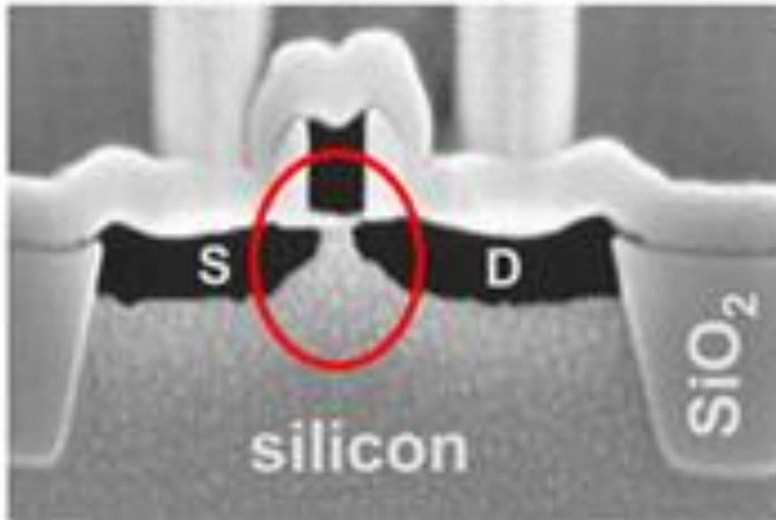
Figura-2.4:
Procesul de fabricatie a unui MOSFET de tip n pe siliciu de tip p.

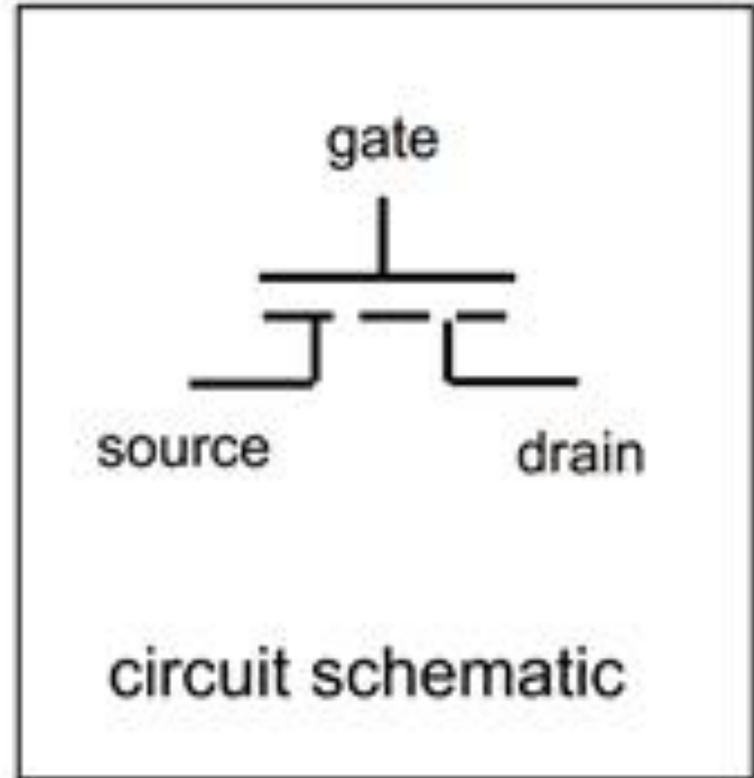






MOS Technology Trends





MICRO FABRICATION CLEANROOM
SCHOOL OF MICROELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS

GOWNING PROCEDURE

1. Put on the Face Mask

2. Put on the Disposable Hair Cover

3. Put on the Coverall
Ensure it does not touch the floor

4. Put on the High Top Booty

5. Swing over to clean area after wearing booty on one side

6. Check in front of mirror

7. Put on Gloves
Ensure the gloves are tight under the garment

8. Enter the air shower room and step on the tacky mat

9. Make a few rotations when air is blown

10. A perfect Cleanroom Gowning

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DEGOWNING PROCEDURE

1. Enter the Air Shower Room

2. Remove the gloves and throw into dustbin

3. Remove one of the high top booties. Swing over to pre-clean area and remove the other high top booty

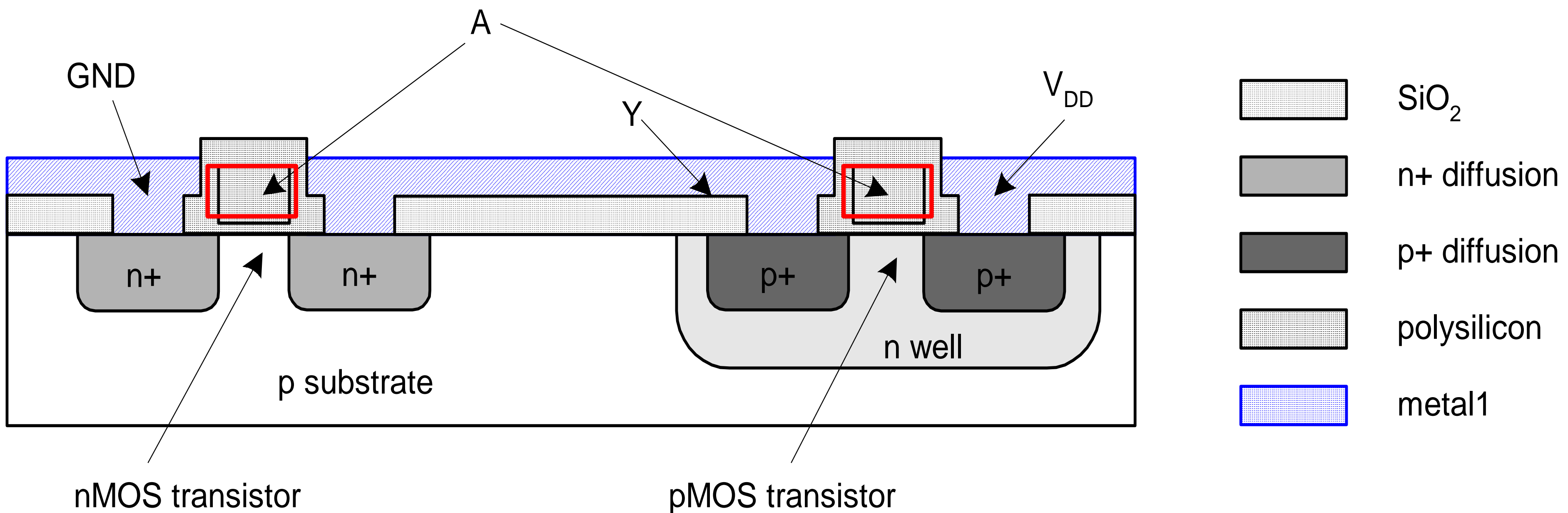
4. Remove the jumpsuit
Ensure it does not touch the floor

Remove the disposable face mask and throw hair cover into dustbin

6. Hang jumpsuit properly in the Garment Cabinet

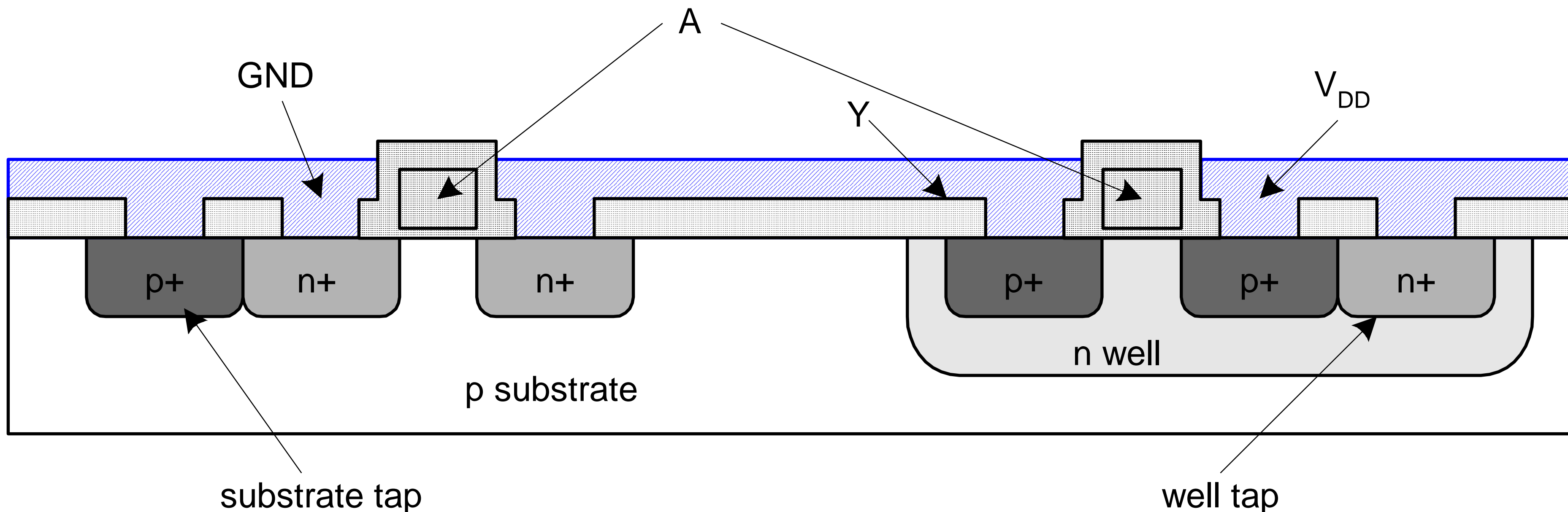
Inverter Cross-section

- Typically use ***p***-type substrate for ***n***MOS transistors
- Requires ***n***-well for body of ***p***MOS transistors



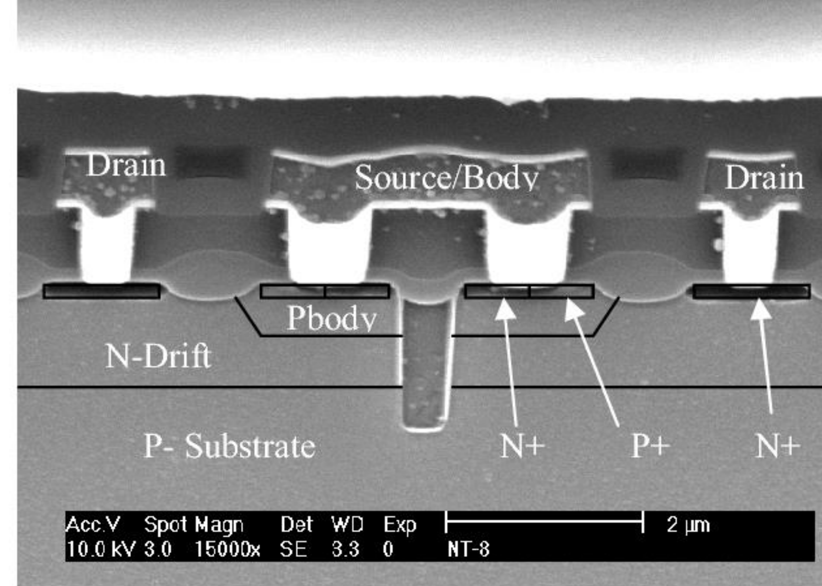
Well and Substrate Taps

- Substrate must be tied to **GND** and ***n***-well to **V_{DD}**
- Metal to lightly-doped semiconductor forms poor connection (used for Schottky Diode)
- Use heavily doped well and substrate contacts / taps



Inverter Mask Set

- Transistors and wires are defined by *masks*
- **Cross-section** taken along **dashed** line



GND

Y

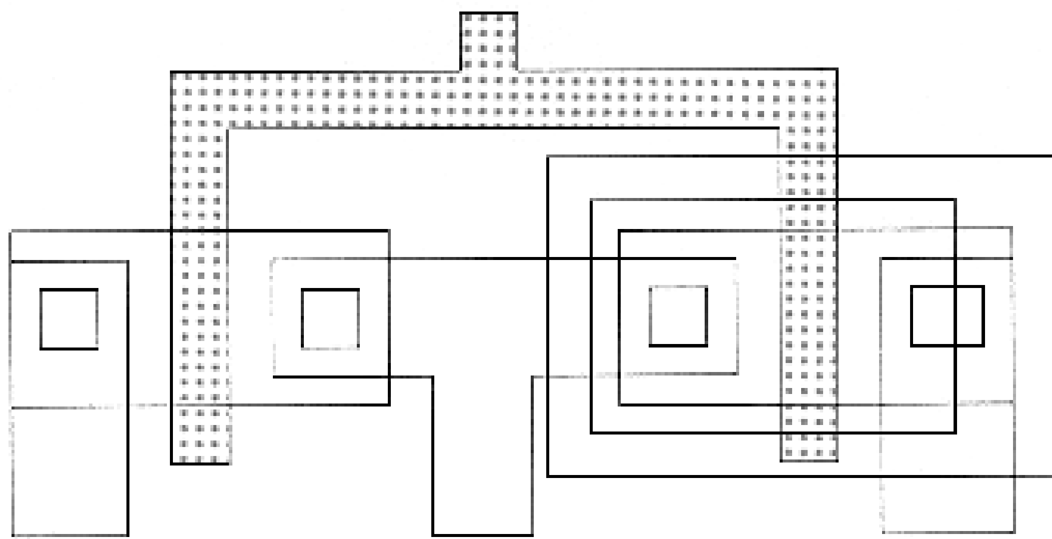
V_{DD}

substrate tap

nMOS transistor

pMOS transistor

well tap



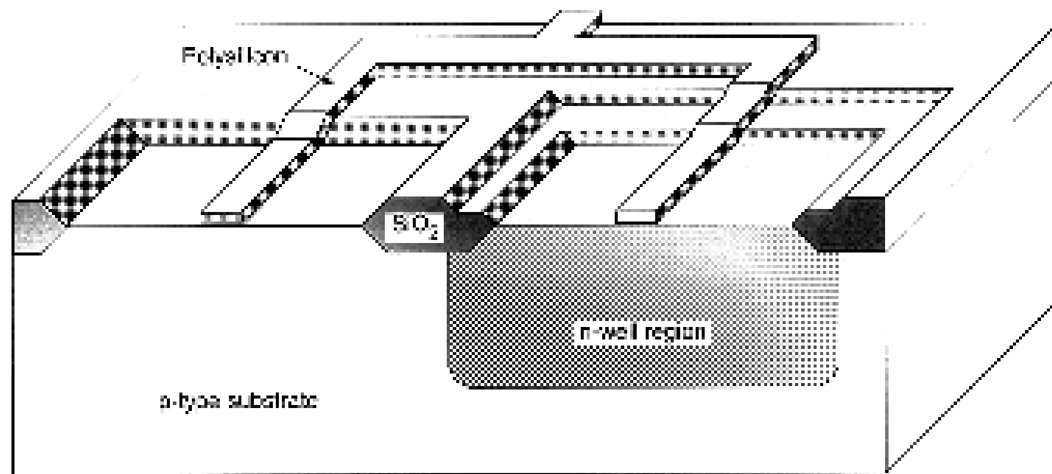


Figura-2.6:
Stratul de polisiliciu este realizat folosind depuneri chimice de vapori (CVD) si format folosind corodarea uscata (cu plasma). Liniile de polisiliciu create vor functiona ca electrozi de poarta pentru tranzistoarele pMOS si nMOS. De asemena, portile de siliciu reprezinta masti cu autoaliniere pentru implantarea sursei si drenei in pasul urmator.

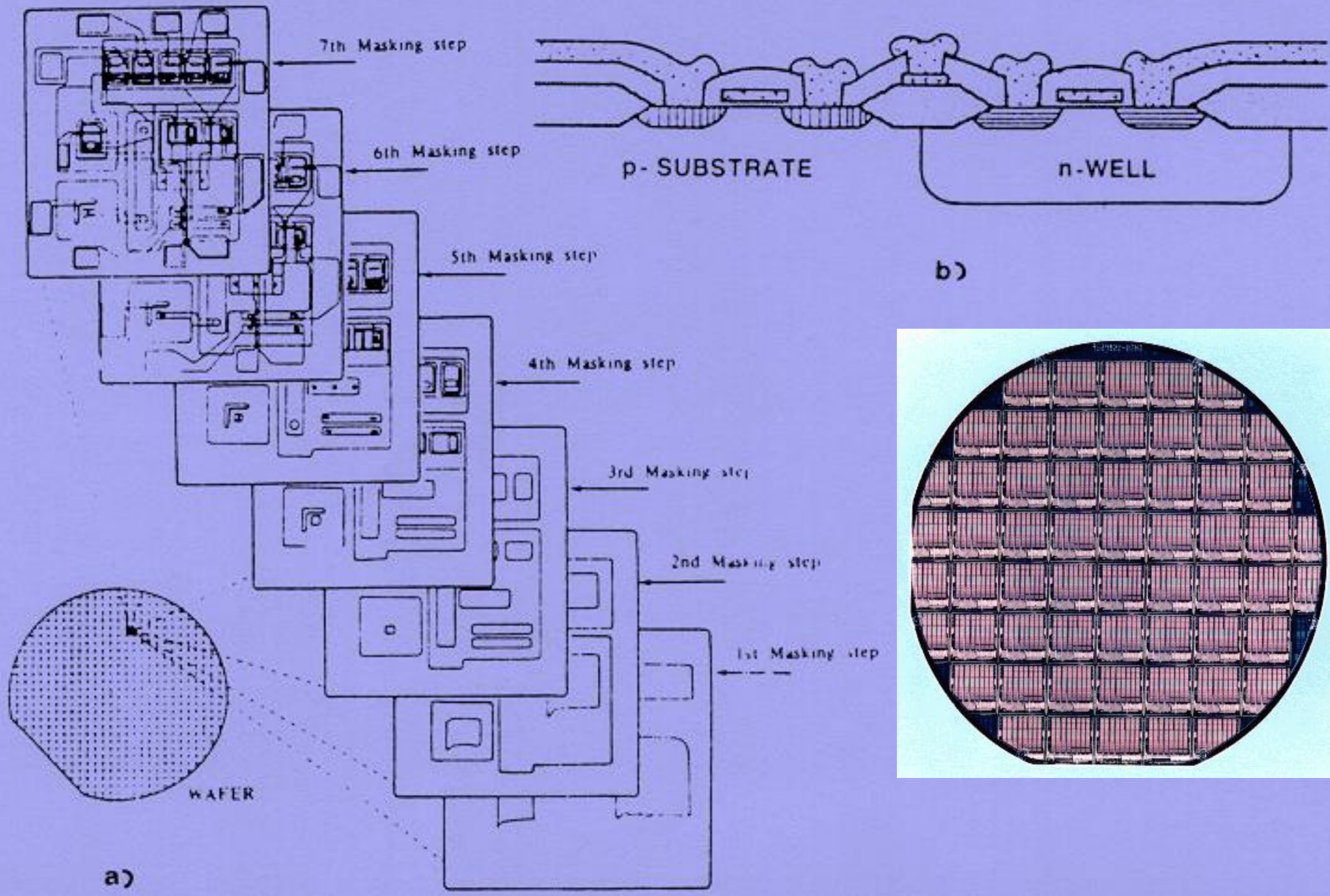
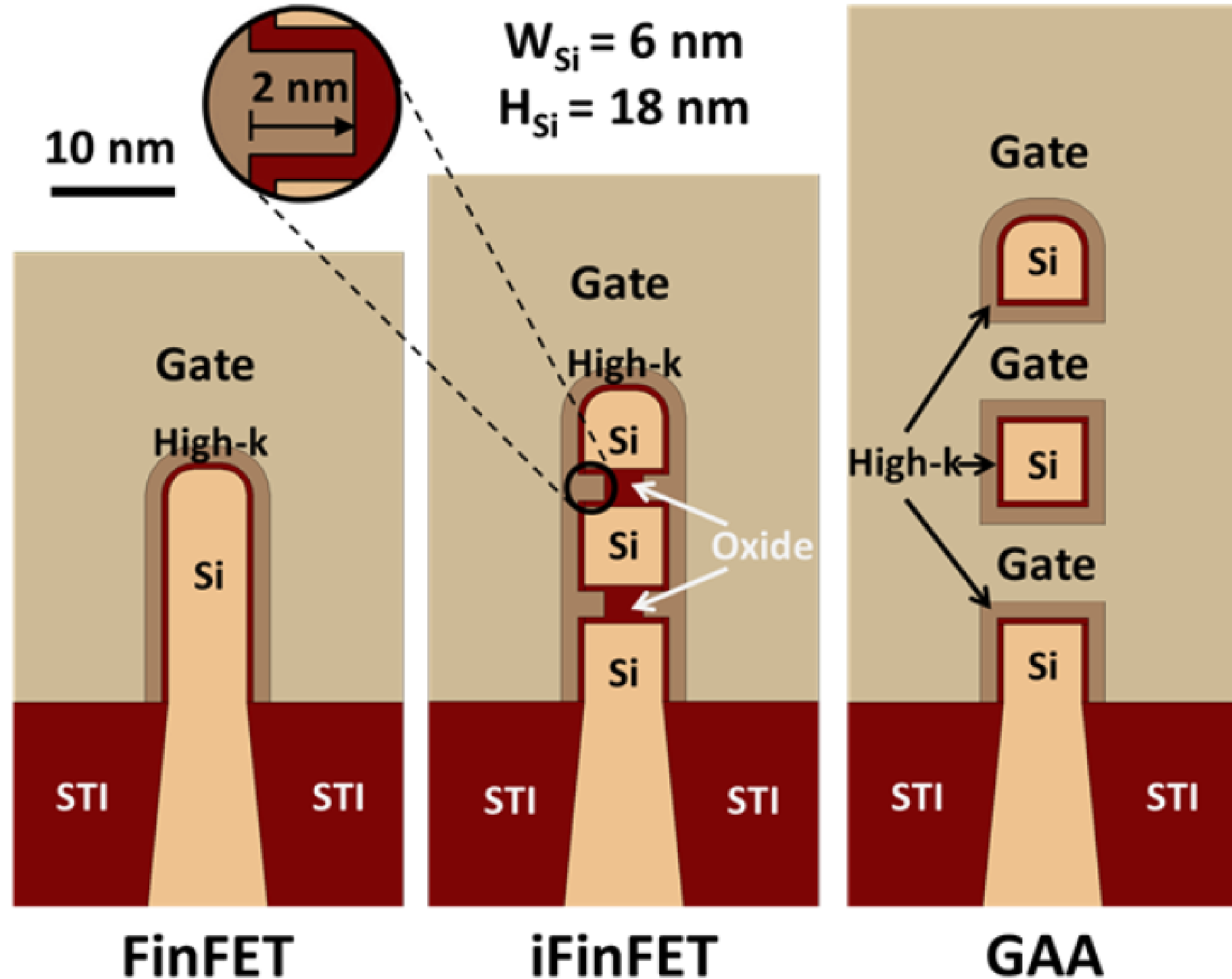


Figura-2.11: Ilustrarea conceptuala a secventei de aplicare a mastilor pentru a crea structurile dorite.

iFinFET Structure and Fabrication

Inserted-Oxide FinFET (iFinFET)

The FinFET structure has been widely adopted at the 14/16 nm generation of CMOS technology.



Cross-sectional views across the fin channel region of multi-gate transistors.