NMOS FABRICATION

The following description explains the basic steps used in the process of fabrication.

(a) The fabrication process starts with the oxidation of the silicon substrate.

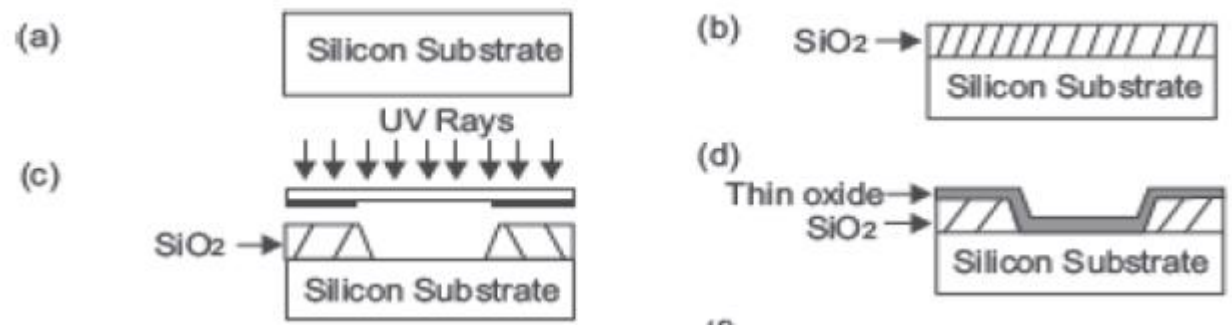
It is shown in the Figure 1.9 (a).

(b) A relatively thick silicon dioxide layer, also called field oxide, is created on the surface of the substrate. This is shown in the Figure 1.9 (b).

(c) Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created. This is indicated in the Figure 1.9 (c).

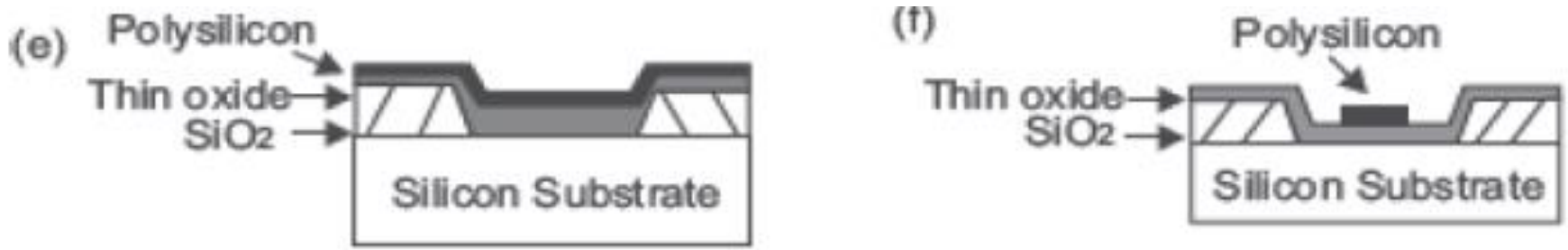
(d) This is followed by covering the surface of substrate with a thin, high-quality oxide layer, which will eventually form the gate oxide of the

MOS transistor as illustrated in Figure 1.9 (d).



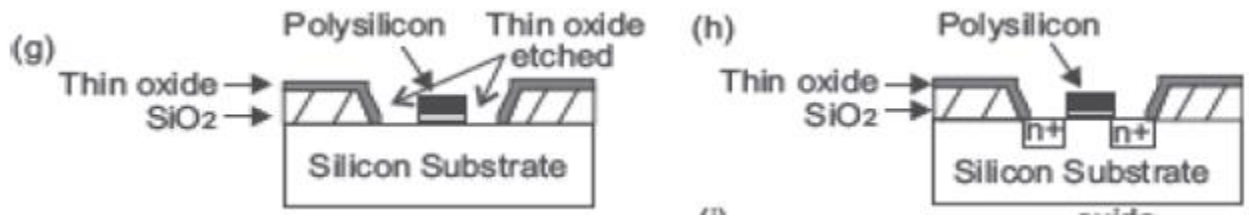
(e) On top of the thin oxide, a layer of polysilicon (polycrystalline silicon) is deposited as is shown in the Figure 1.9 (e). Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

(f) After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates. This is shown in Figure 1.9 (f).



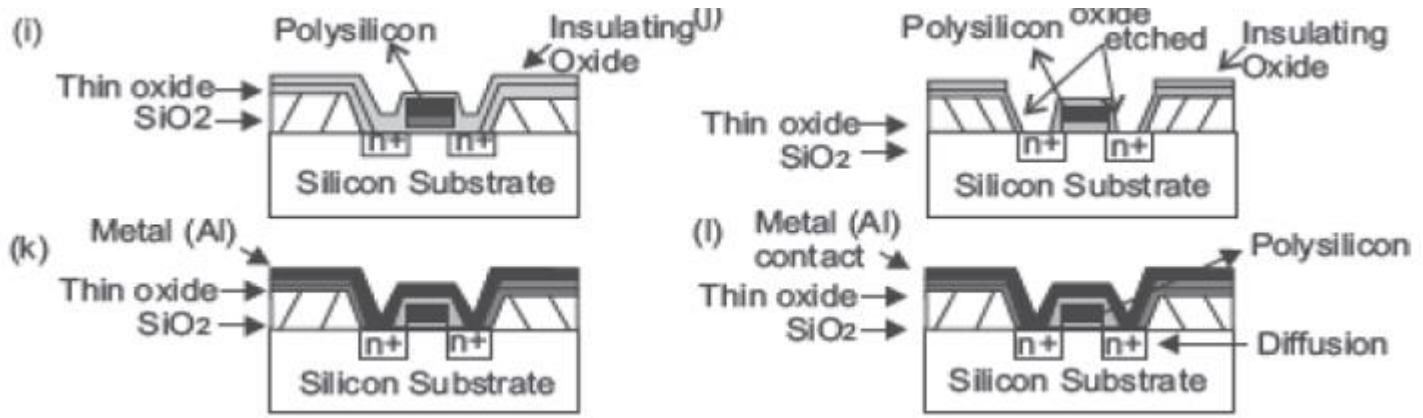
(g) The thin gate oxide not covered by polysilicon is also etched along, which exposes the bare silicon surface on which the source and drain junctions are to be formed (Figure 1.9 (g)).

(h) The entire silicon surface is then doped with high concentration of impurities, either through diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Diffusion is achieved by heating the wafer to a high temperature and passing the gas containing desired impurities over the surface. Figure 1.9 (h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.



(i) Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide, as shown in

Figure 1.9 (i).(*j*) The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions, as illustrated in Figure 1.9 (j).



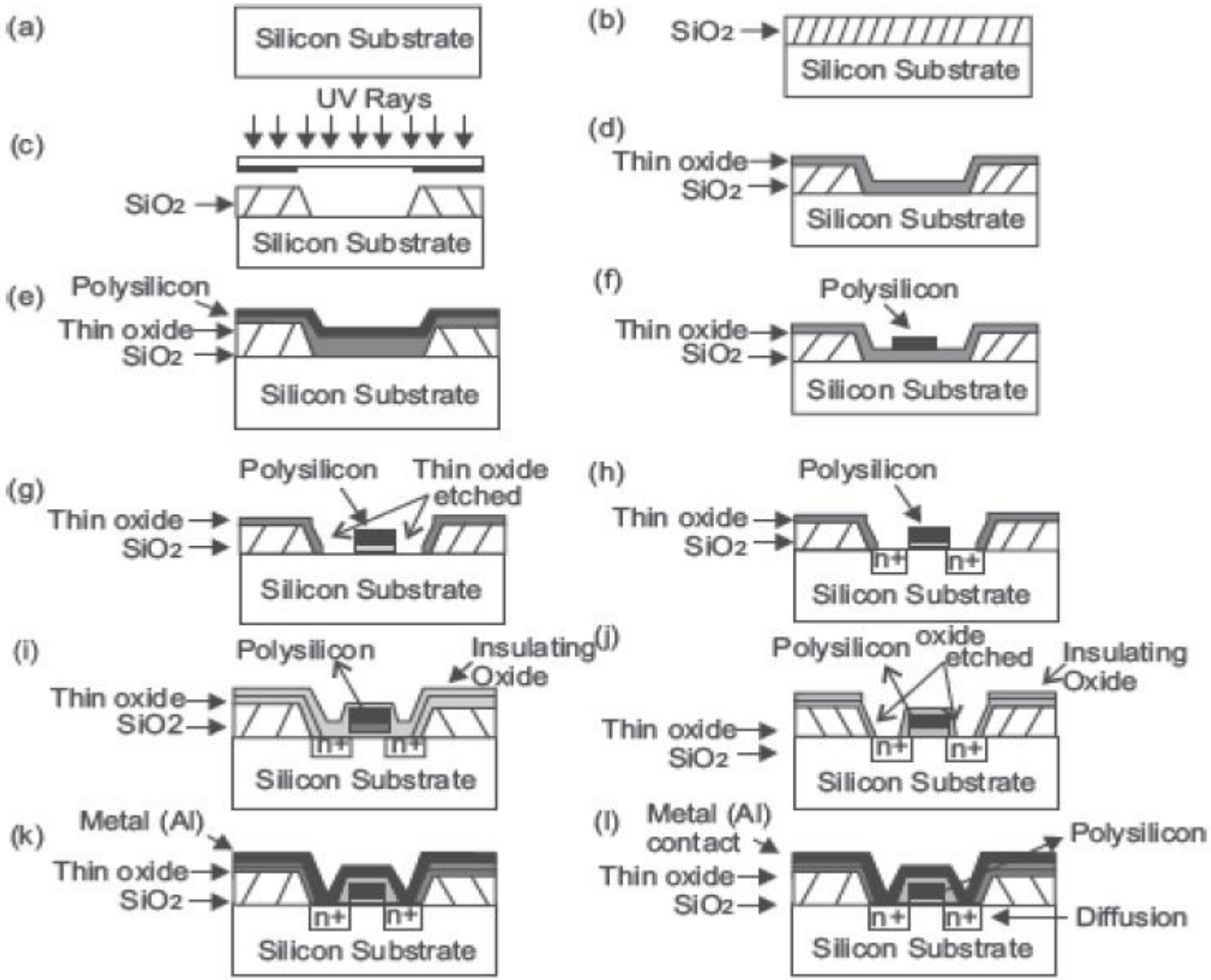
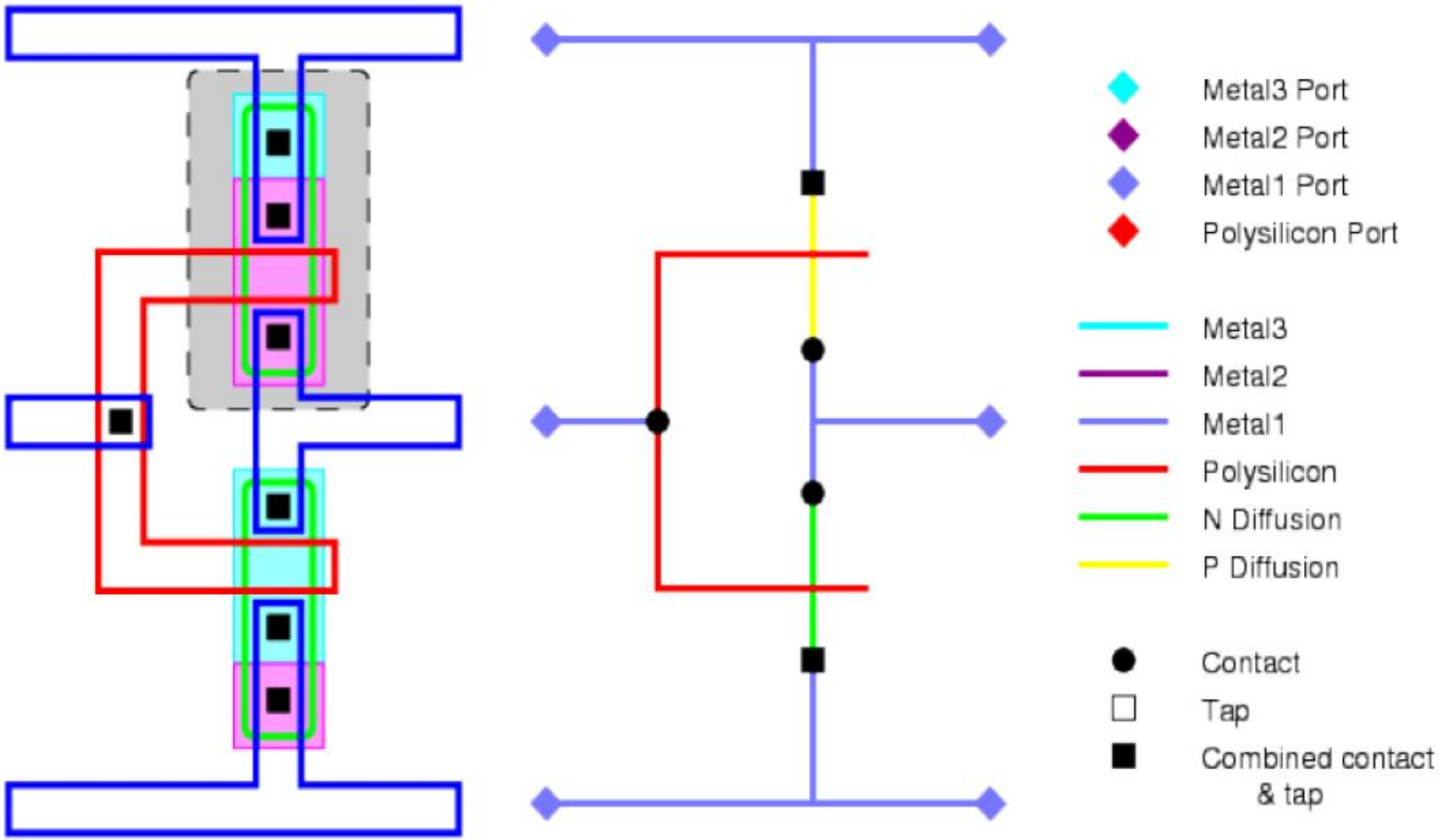


Figure 1.9: Fabrication Process of NMOS Device

Layout & Stick Diagram of CMOS Inverter



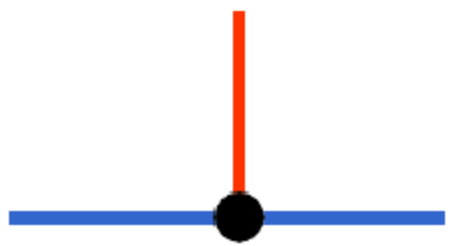
Stick Diagrams – Some Rules

Rule 1:

When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.

Rule 2:

When two or more “sticks” of different type cross or touch each other there is no electrical contact. (If electrical contact is needed we have to show the connection explicitly)



Rule 3:

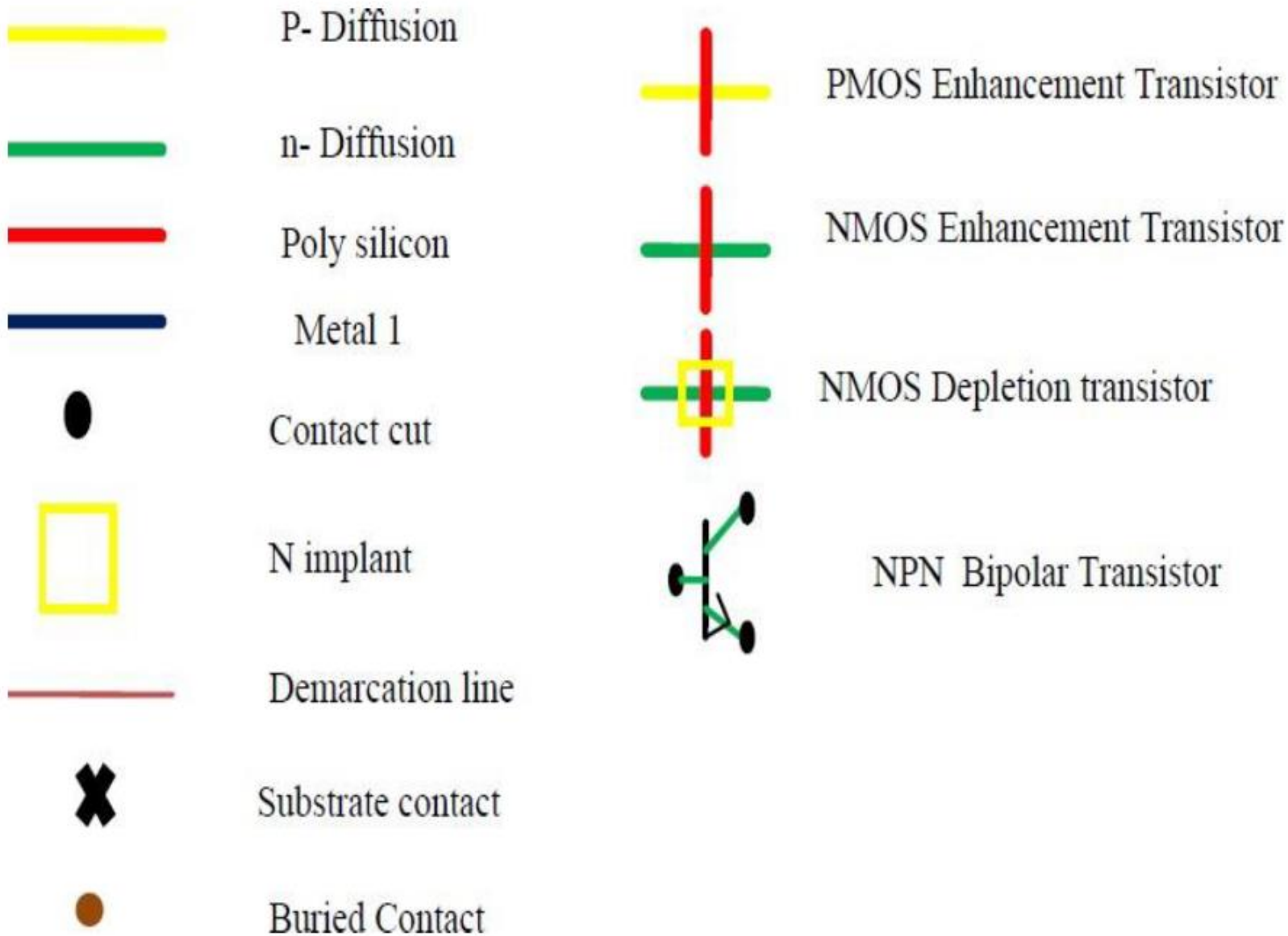
When a poly crosses diffusion it represents a transistor.

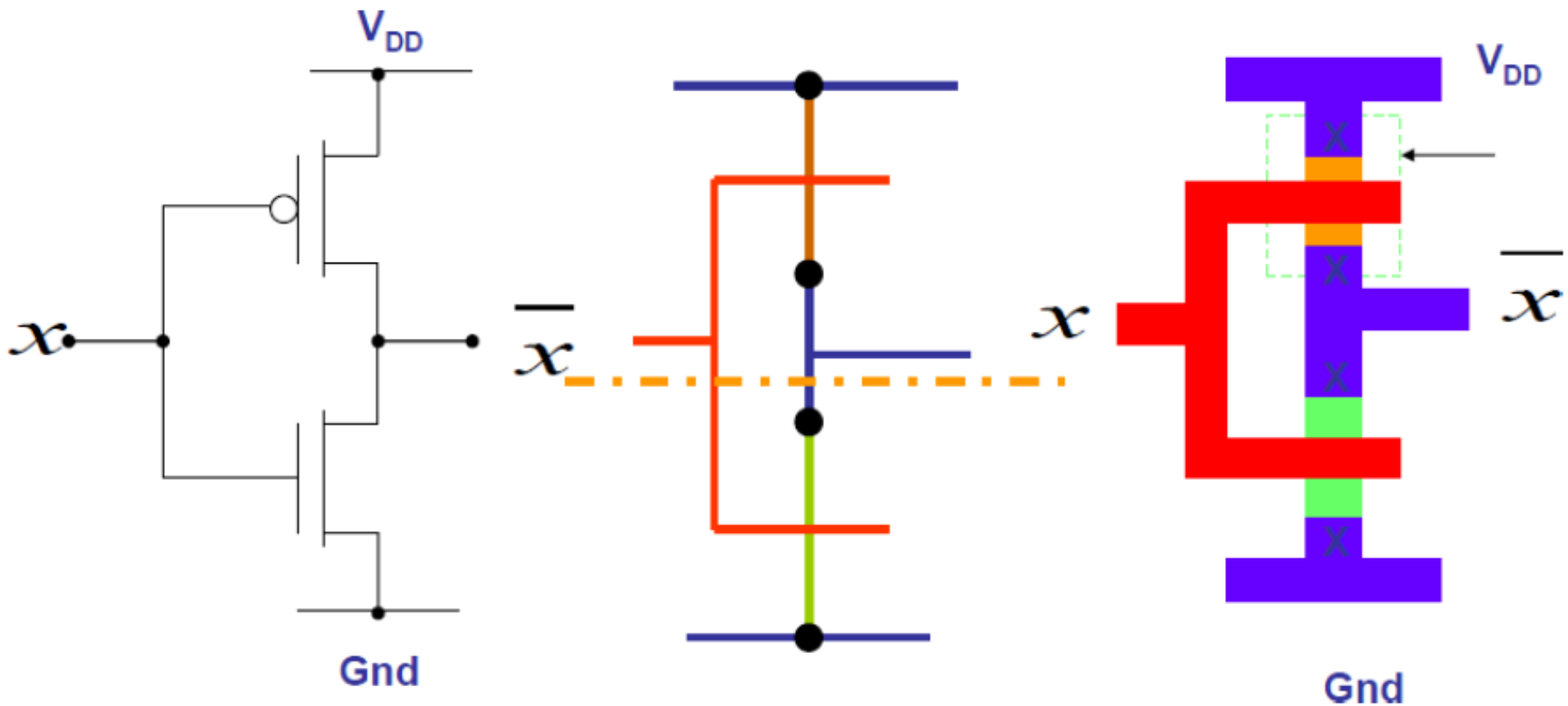
Note: If a contact is shown then it is ***not*** a transistor.

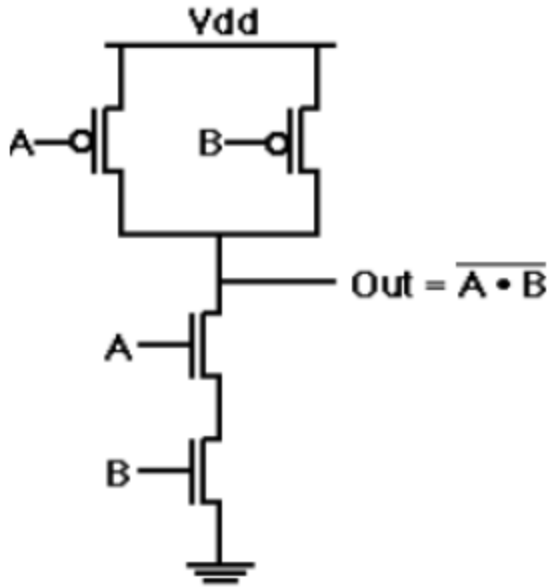
Rule 4:

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

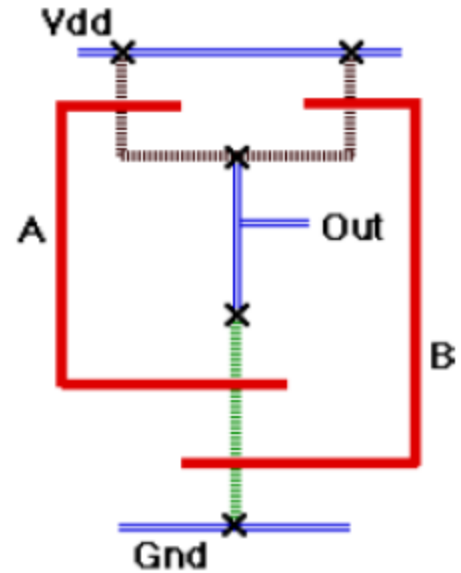
Stick Diagrams:




V_{DD}
x
$\overline{x}$
Gnd
x
V_{DD}
$\overline{x}$
Gnd



A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0



1. Pull-down: Connect to ground If A=1 AND B=1

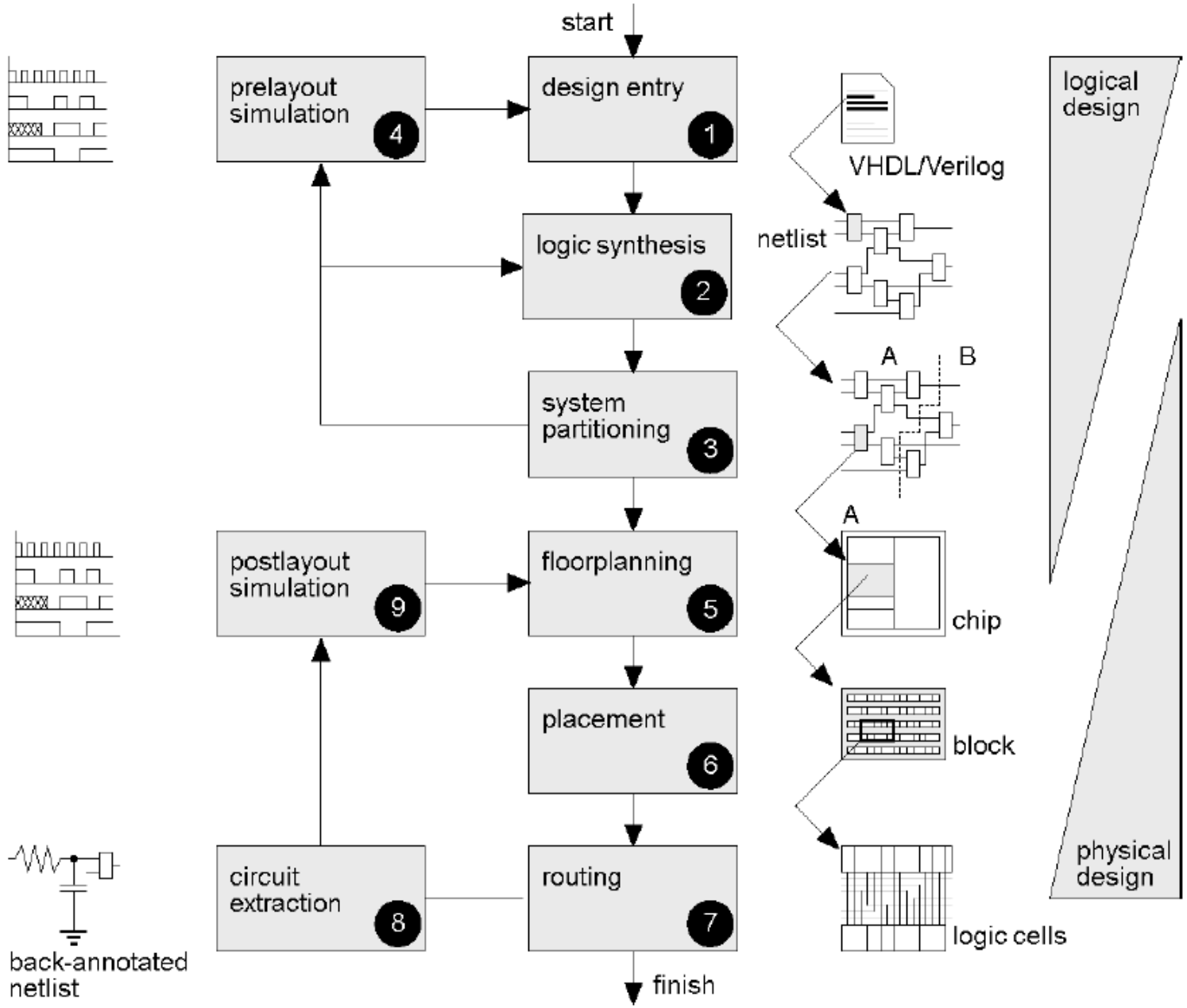
2. Pull-up: Connect to Vdd If A=0 OR B=0

Fig. CMOS NAND gate

LAMBDA BSED RULES

MINIMUM WIDTH AND SPACING RULES

LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
N/P DIFFUSION	Minimum Width Minimum Spacing	3λ 3λ
N-WELL	Minimum Width Minimum Spacing	3λ 3λ
P-WELL	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ


start
prelayout simulation
4
design entry
1
logic synthesis
2
system partitioning
3
floorplanning
5
placement
6
routing
7
circuit extraction
8
postlayout simulation
9
finish
VHDL/Verilog
netlist
A
B
A
chip
block
logic cells
logical design
physical design
back-annotated netlist