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# Simplified Example of a LOCOS Fabrication Process

# LOCOS Defined

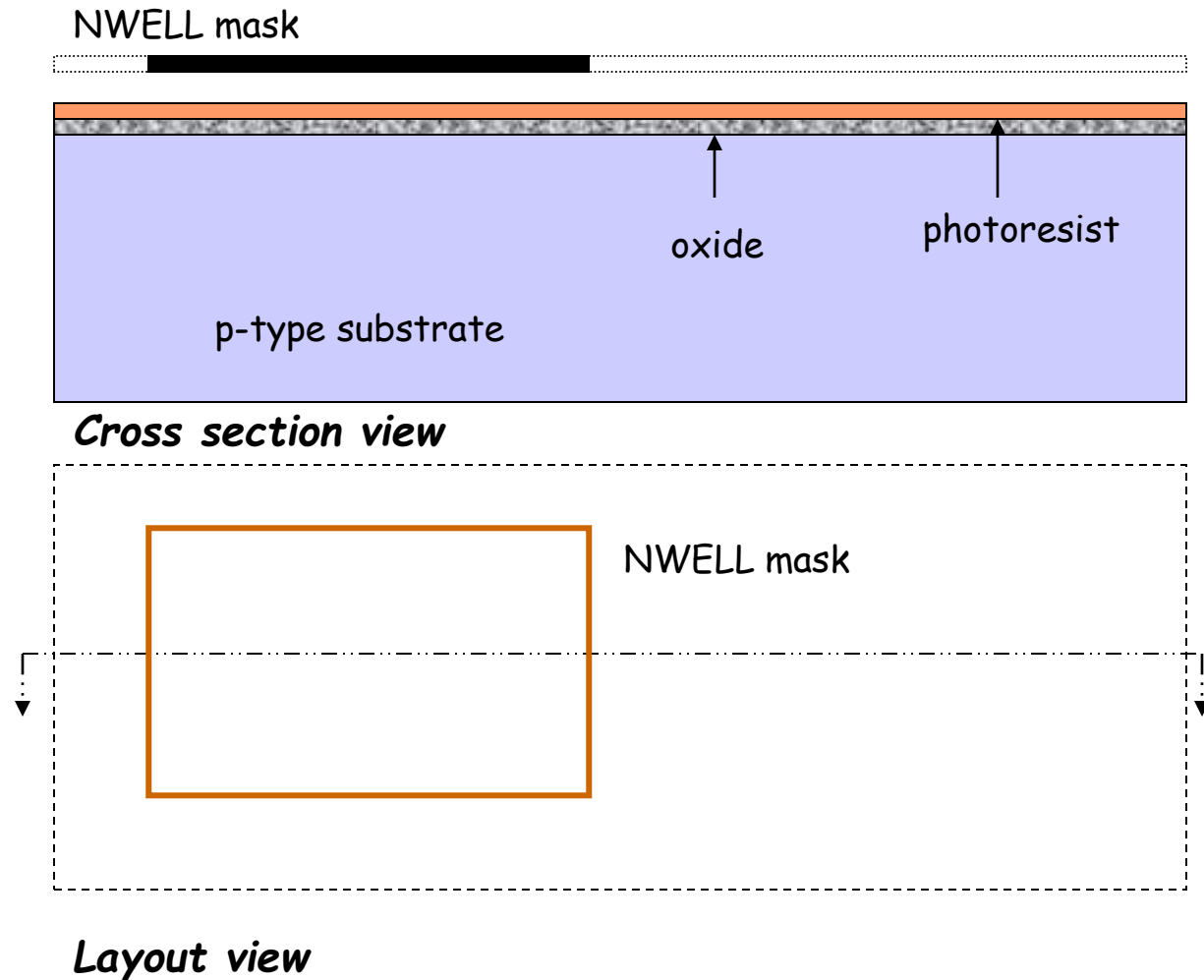
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- LOCOS = LOCAL Oxidation of Silicon
- Defines a set of fabrication technologies where
  - the wafer is masked to cover all active regions
  - thick field oxide (FOX) is grown in all non-active regions
- Used for electrical isolation of CMOS devices
- Relatively simple to understand so often used to introduce/describe CMOS fabrication flows
- Not commonly used in modern fabrication
  - other techniques, such as Shallow Trench Isolation (STI) are currently more common than LOCOS

# LOCOS -step 1

## Form N-Well regions

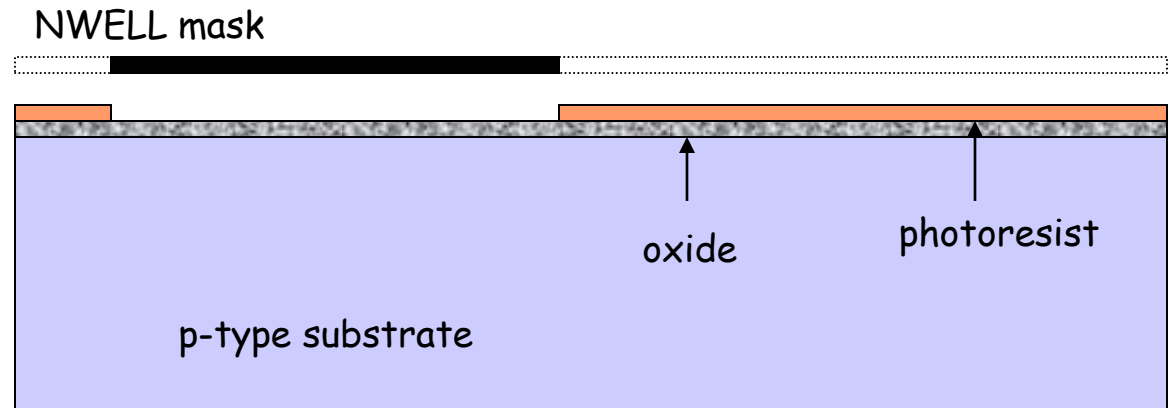
- Grow oxide
- Deposit photoresist



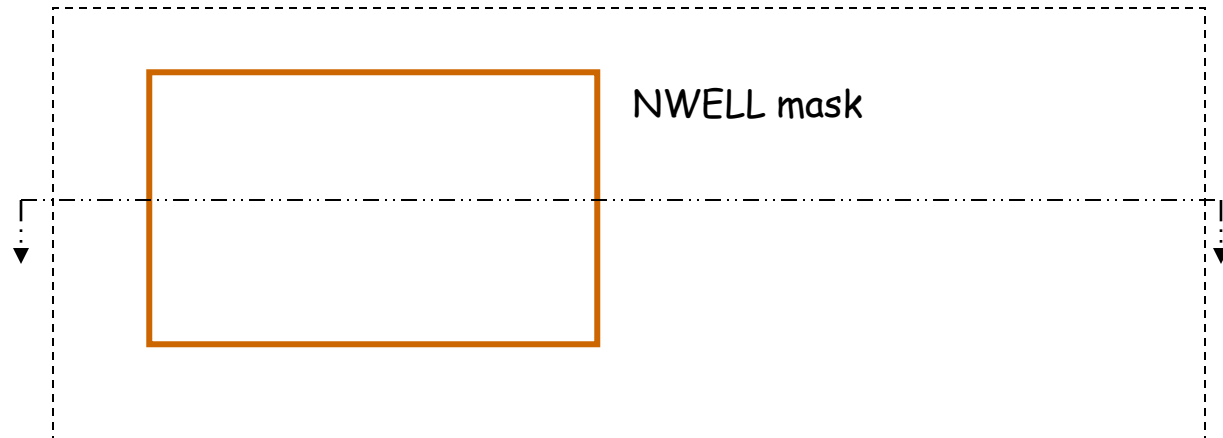
# LOCOS -step 1

## Form N-Well regions

- Grow oxide
- Deposit photoresist
- Pattern photoresist
  - NWELL Mask
  - expose only n-well areas



*Cross section view*

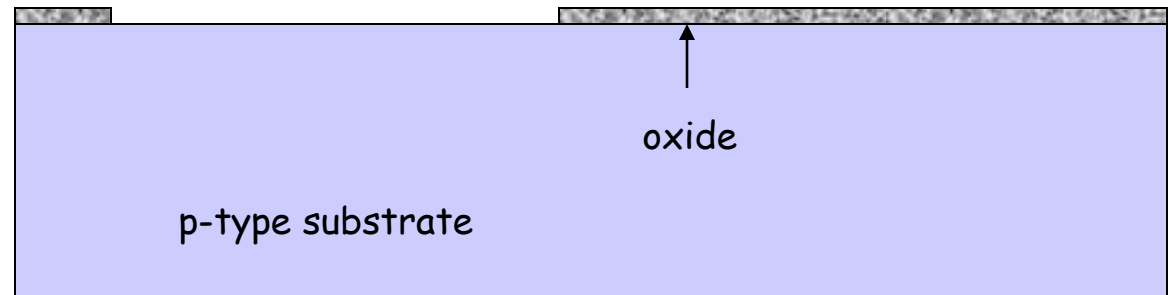


*Layout view*

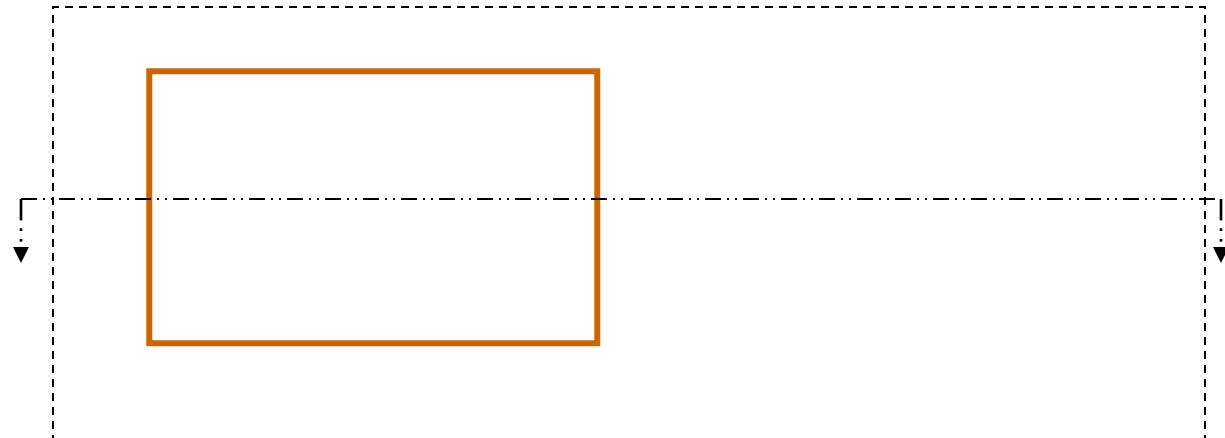
# LOCOS -step 1

## Form N-Well regions

- Grow oxide
- Deposit photoresist
- Pattern photoresist
  - NWELL Mask
  - expose only n-well areas
- Etch oxide
- Remove photresist



*Cross section view*

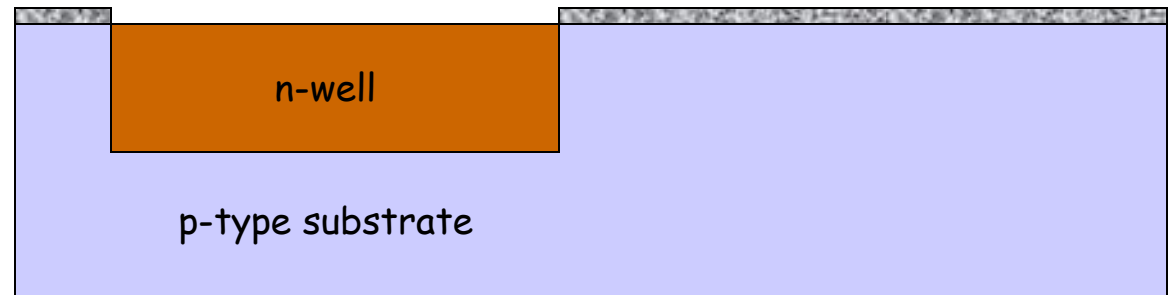


*Layout view*

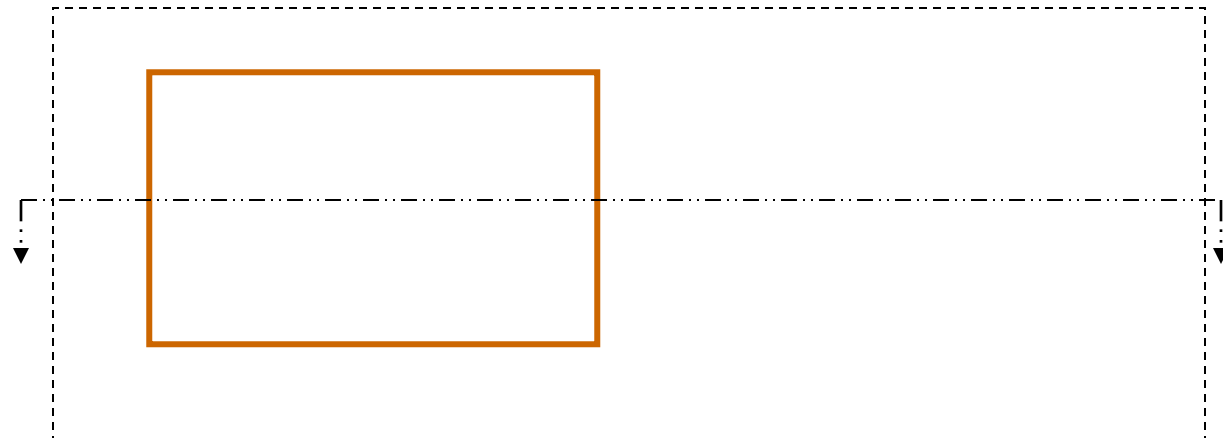
# LOCOS -step 1

## Form N-Well regions

- Grow oxide
- Deposit photoresist
- Pattern photoresist
  - NWELL Mask
  - expose only n-well areas
- Etch oxide
- Remove photoresist
- Diffuse n-type dopants through oxide mask layer



*Cross section view*

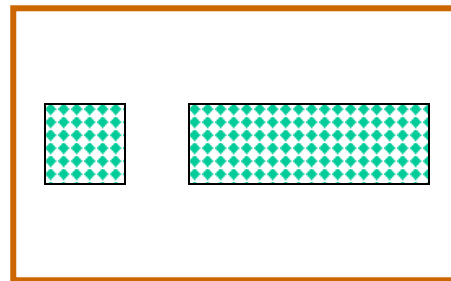
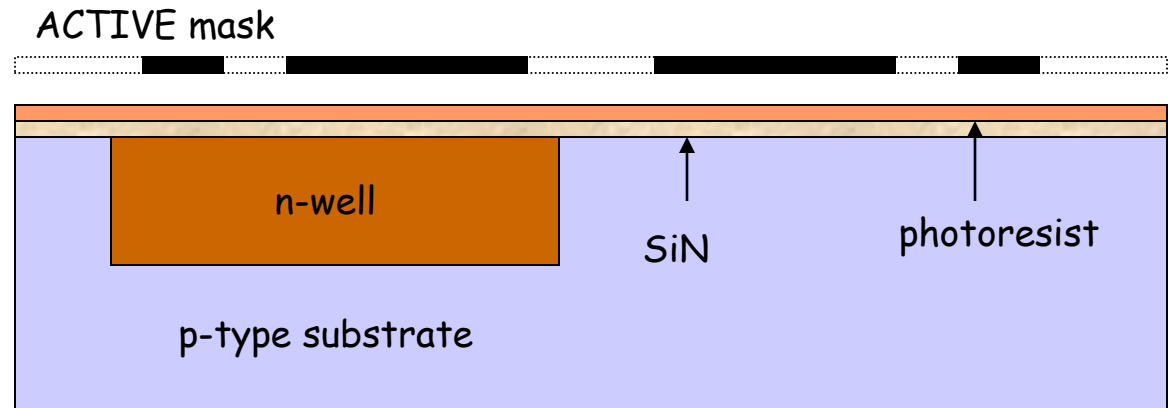


*Layout view*

# LOCOS -step 2

## Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer

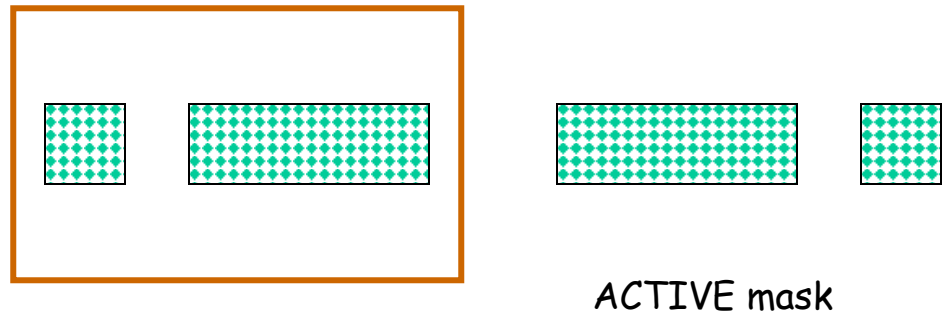
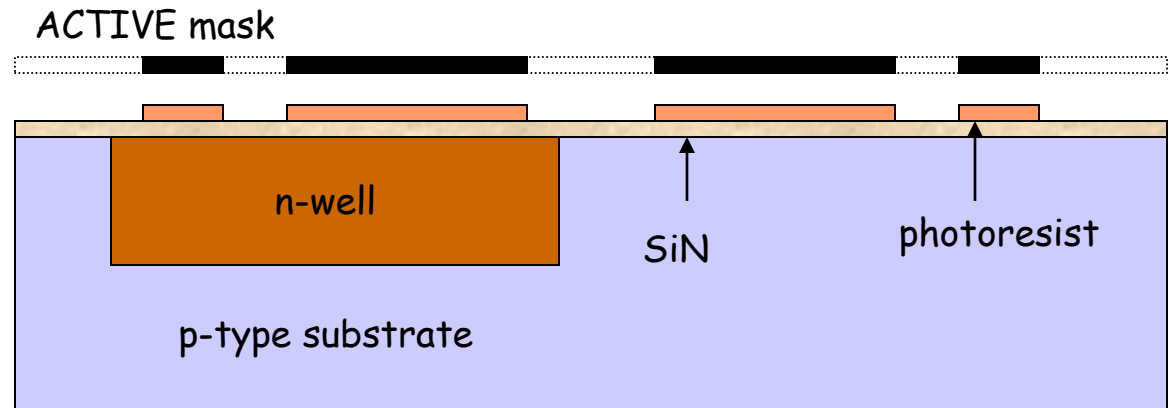


ACTIVE mask

# LOCOS -step 2

## Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer
- Pattern photoresist
  - \*ACTIVE MASK

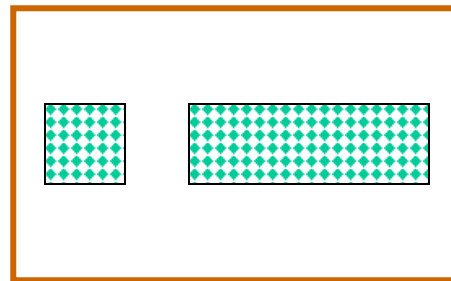
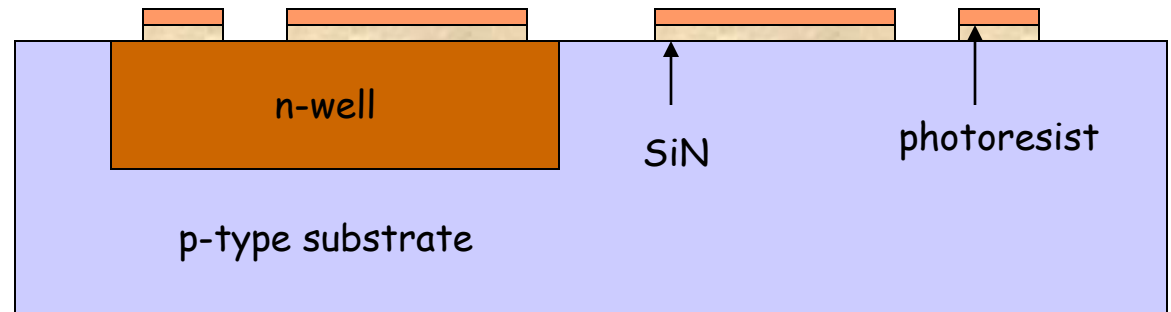




# LOCOS -step 2

## Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer
- Pattern photoresist
  - \*ACTIVE MASK
- Etch SiN in exposed areas
  - leaves SiN mask which blocks oxide growth

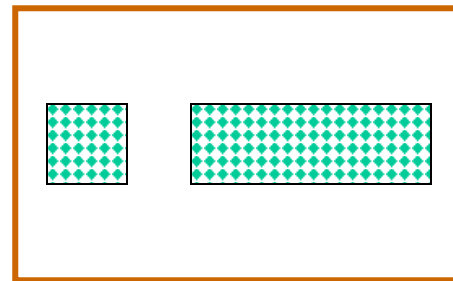
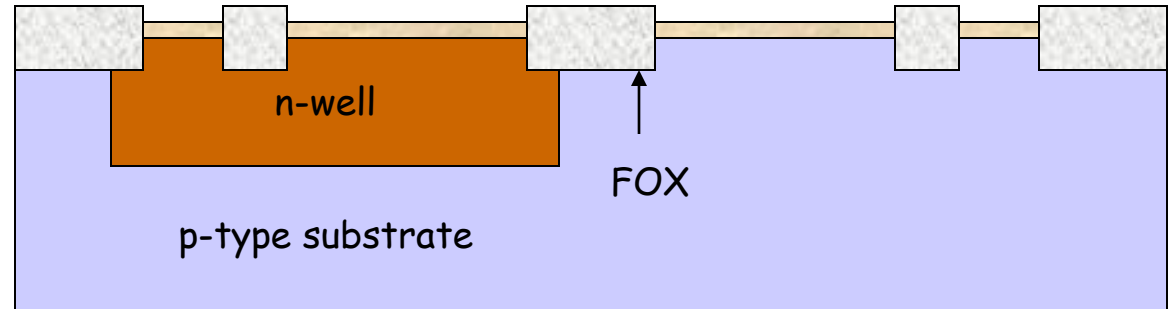


ACTIVE mask

# LOCOS -step 2

## Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer
- Pattern photoresist
  - \*ACTIVE MASK
- Etch SiN in exposed areas
  - leaves SiN mask which blocks oxide growth
- Remove photoresist
- Grow Field Oxide (FOX)
  - thermal oxidation

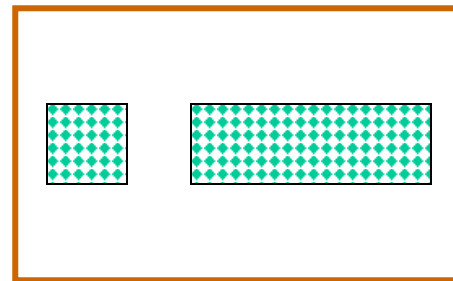
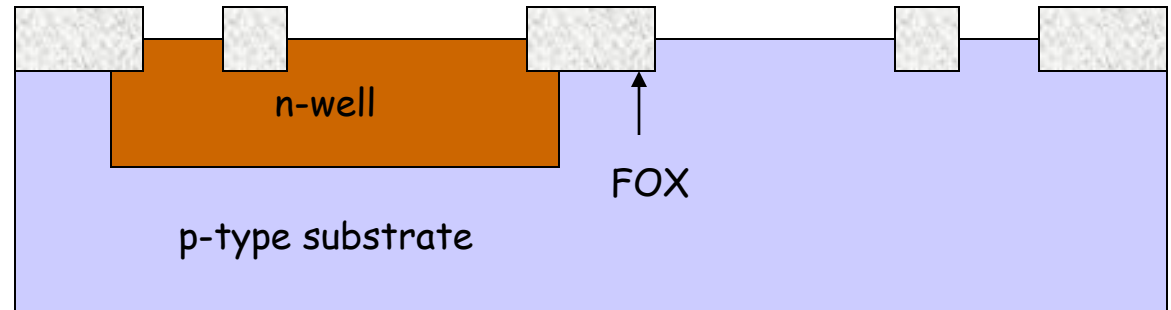


ACTIVE mask

# LOCOS -step 2

## Form Active Regions

- Deposit SiN over wafer
- Deposit photoresist over SiN layer
- Pattern photoresist
  - \*ACTIVE MASK
- Etch SiN in exposed areas
  - leaves SiN mask which blocks oxide growth
- Remove photoresist
- Grow Field Oxide (FOX)
  - thermal oxidation
- Remove SiN

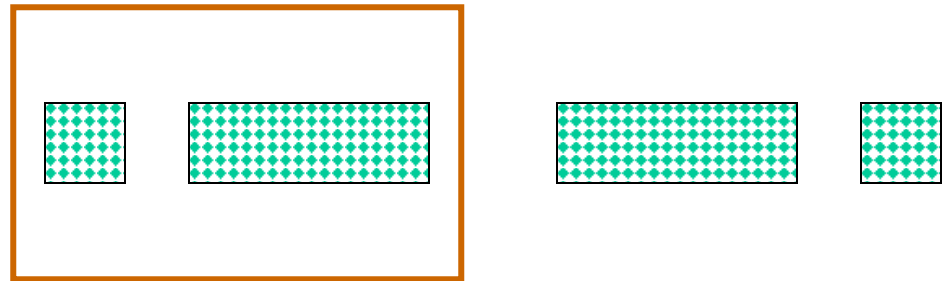
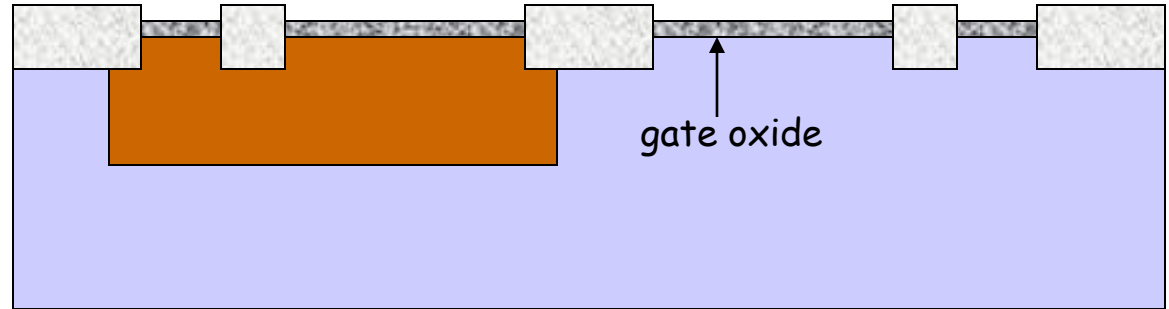


ACTIVE mask

# LOCOS -step 3

## Form Gate (Poly layer)

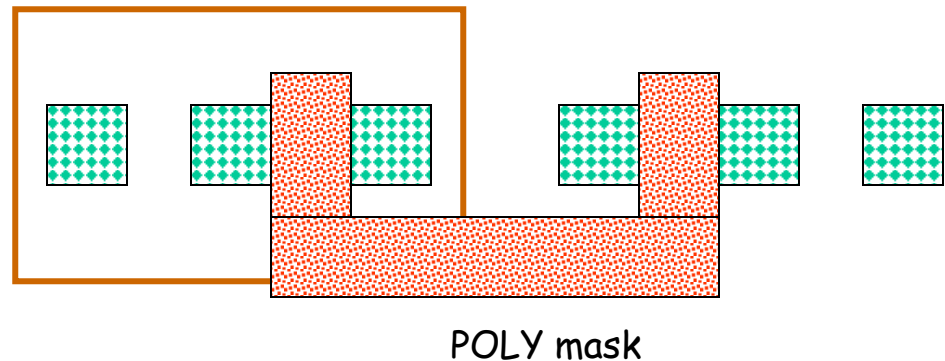
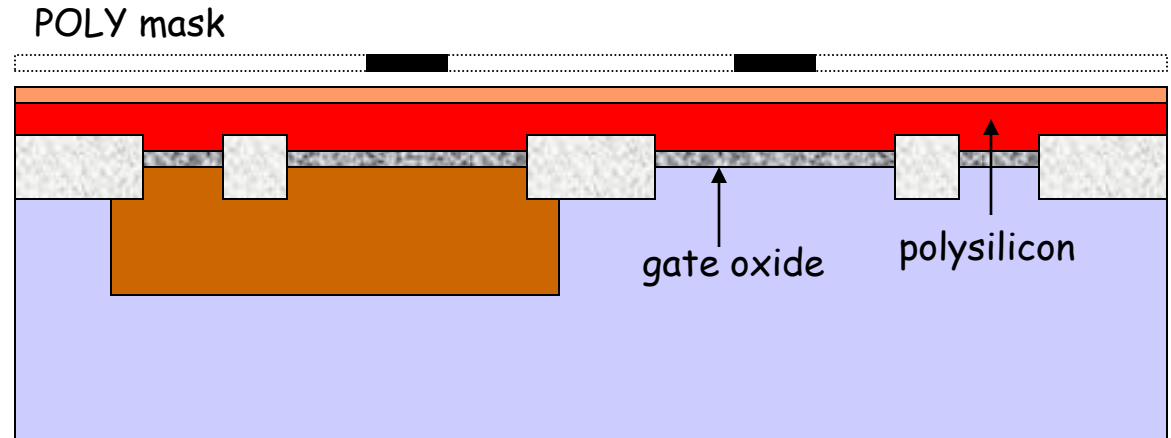
- Grow thin Gate Oxide
  - over entire wafer
  - negligible effect on FOX regions



# LOCOS -step 3

## Form Gate (Poly layer)

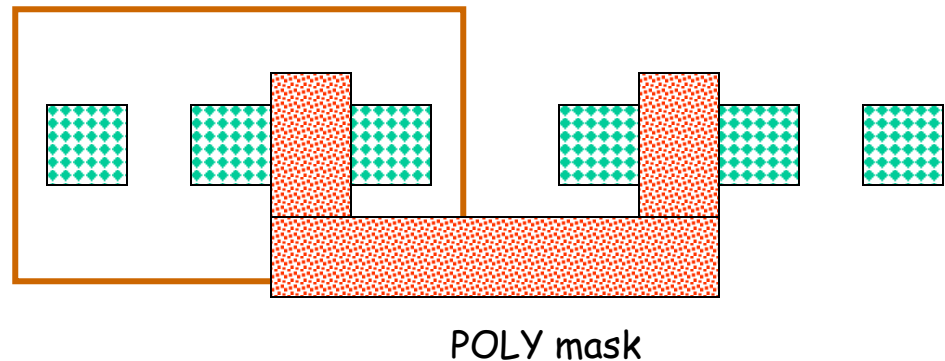
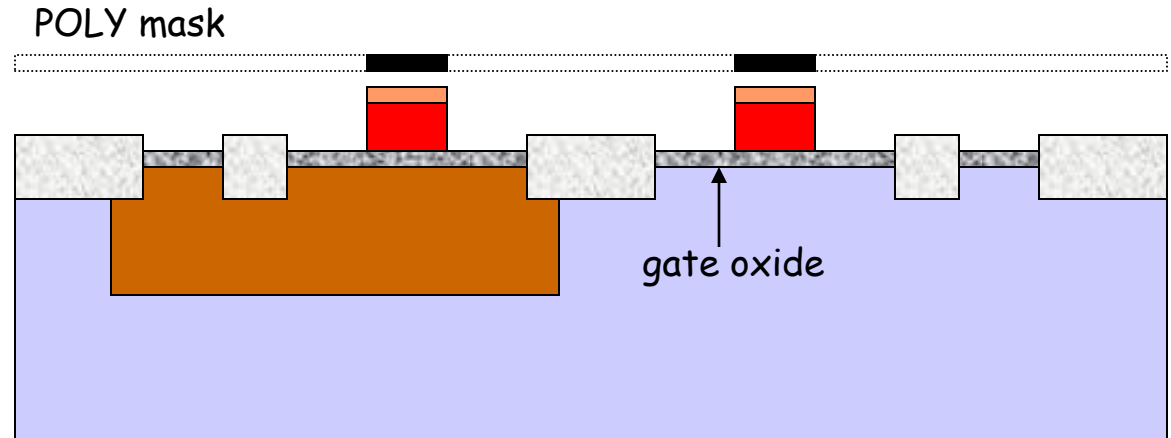
- Grow thin Gate Oxide
  - over entire wafer
  - negligible effect on FOX regions
- Deposit Polysilicon
- Deposit Photoresist



# LOCOS -step 3

## Form Gate (Poly layer)

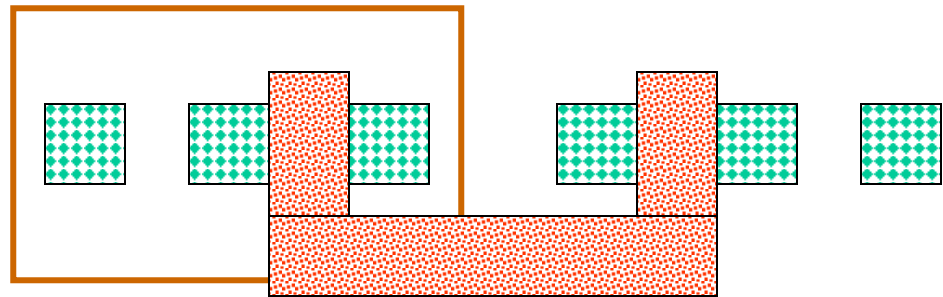
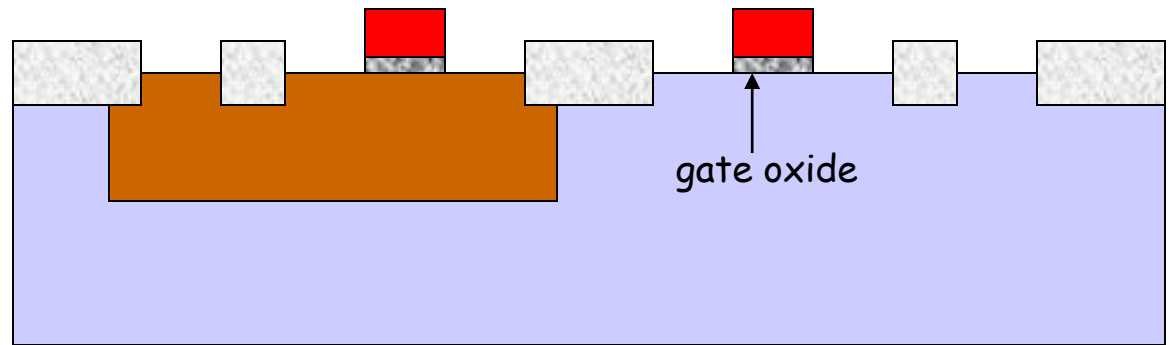
- Grow thin Gate Oxide
  - over entire wafer
  - negligible effect on FOX regions
- Deposit Polysilicon
- Deposit Photoresist
- Pattern Photoresist
  - \*POLY MASK
- Etch Poly in exposed areas
- Etch/remove Oxide
  - gate protected by poly



# LOCOS -step 3

## Form Gate (Poly layer)

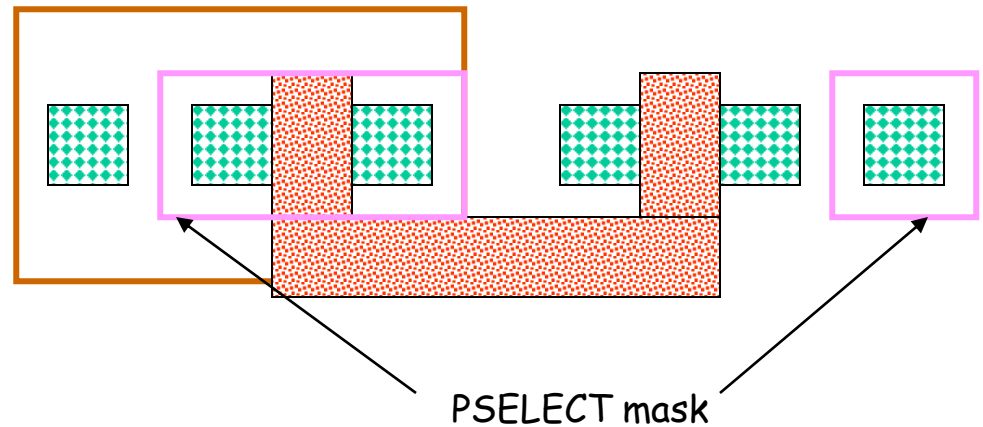
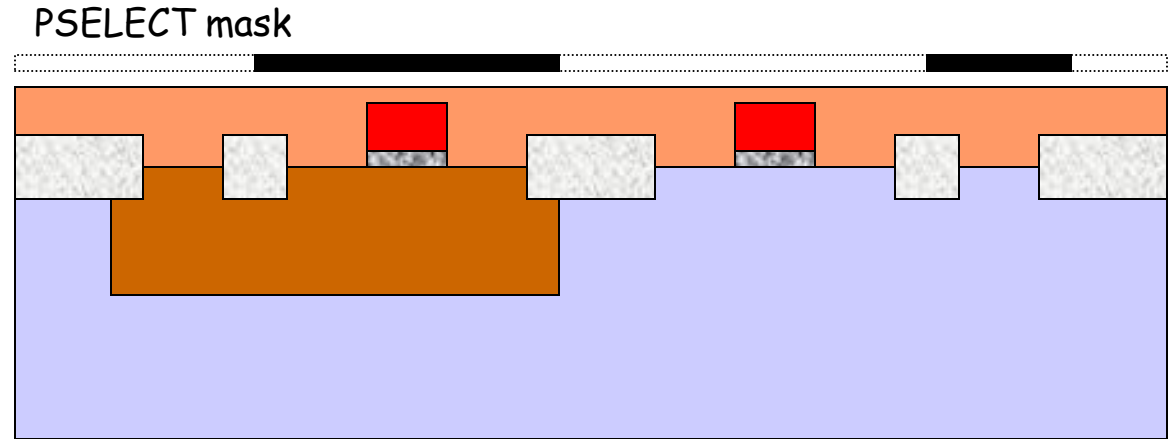
- Grow thin Gate Oxide
  - over entire wafer
  - negligible effect on FOX regions
- Deposit Polysilicon
- Deposit Photoresist
- Pattern Photoresist
  - \*POLY MASK
- Etch Poly in exposed areas
- Etch/remove Oxide
  - gate protected by poly



# LOCOS -step 4

## Form pmos S/D

- Cover with photoresist

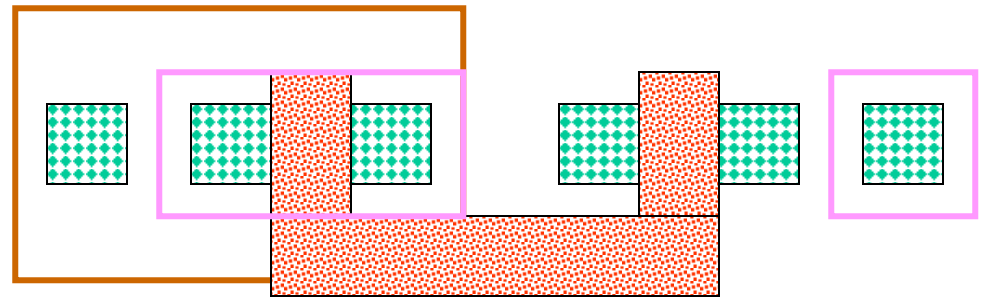
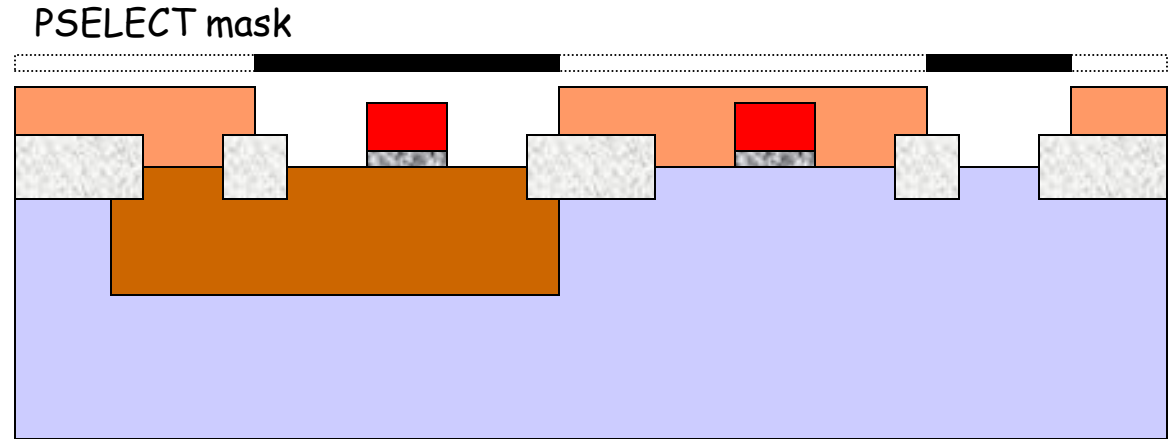




# LOCOS -step 4

## Form pmos S/D

- Cover with photoresist
- Pattern photoresist
  - \*PSELECT MASK

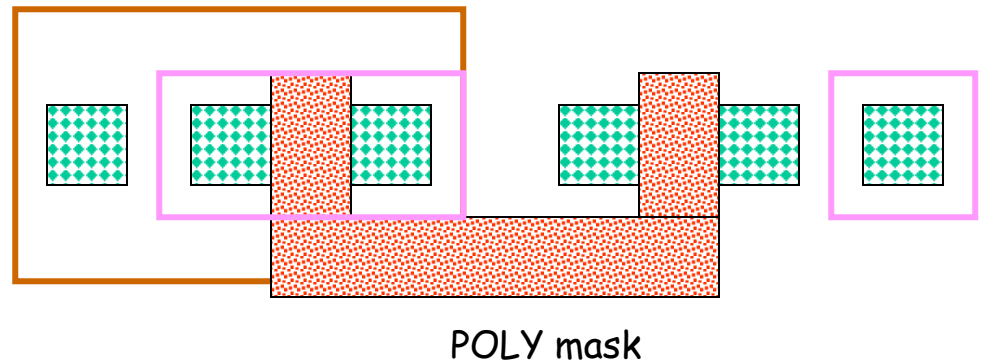
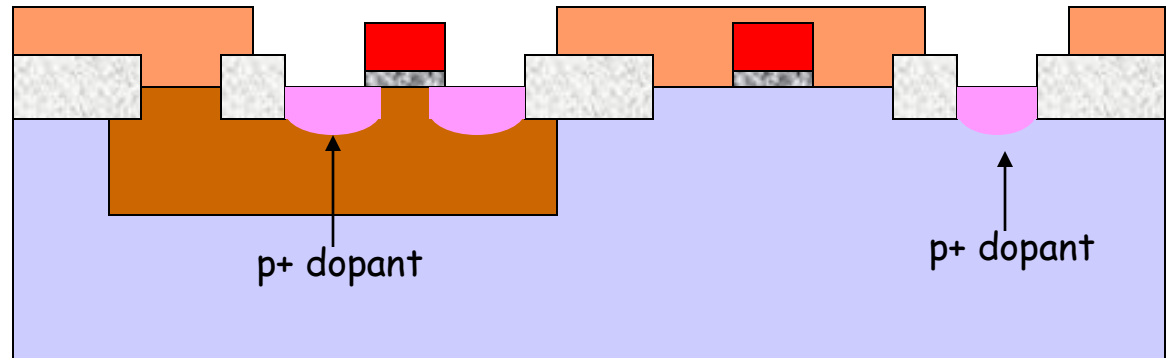


POLY mask

# LOCOS -step 4

## Form pmos S/D

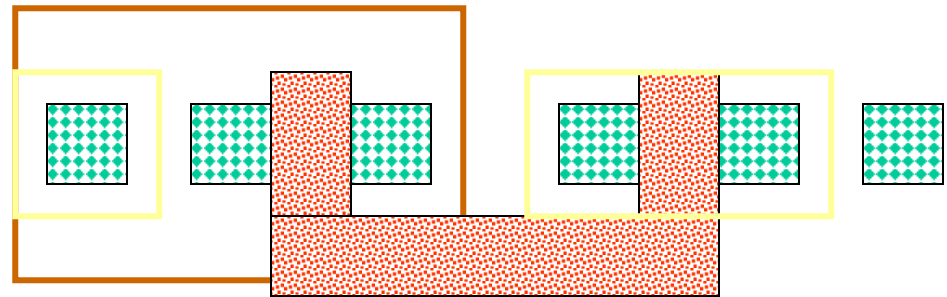
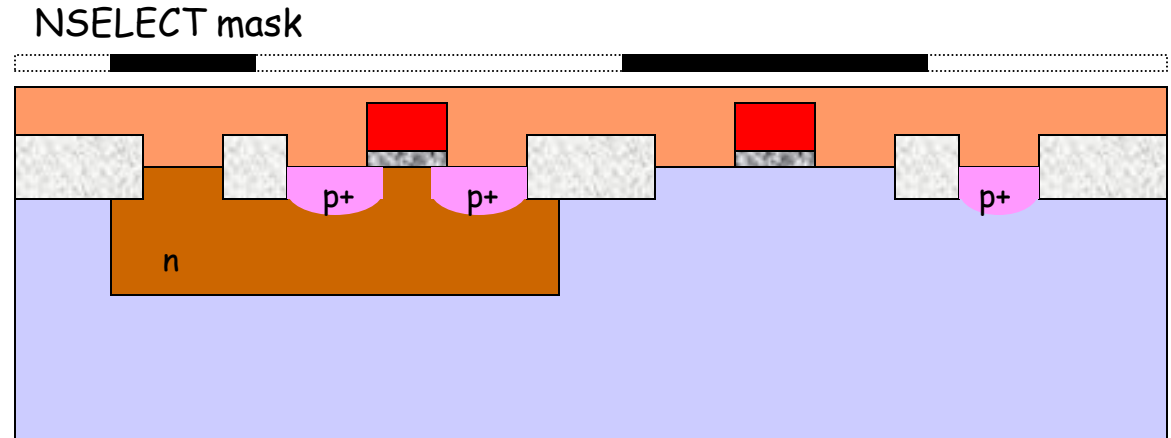
- Cover with photoresist
- Pattern photoresist
  - \*PSELECT MASK
- Implant p-type dopants
- Remove photoresist



# LOCOS -step 5

## Form nmos S/D

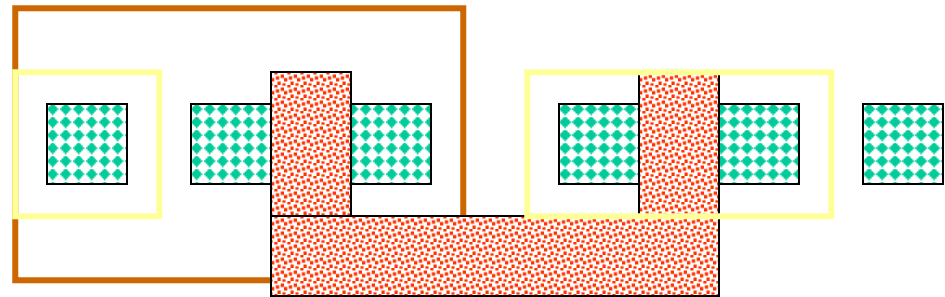
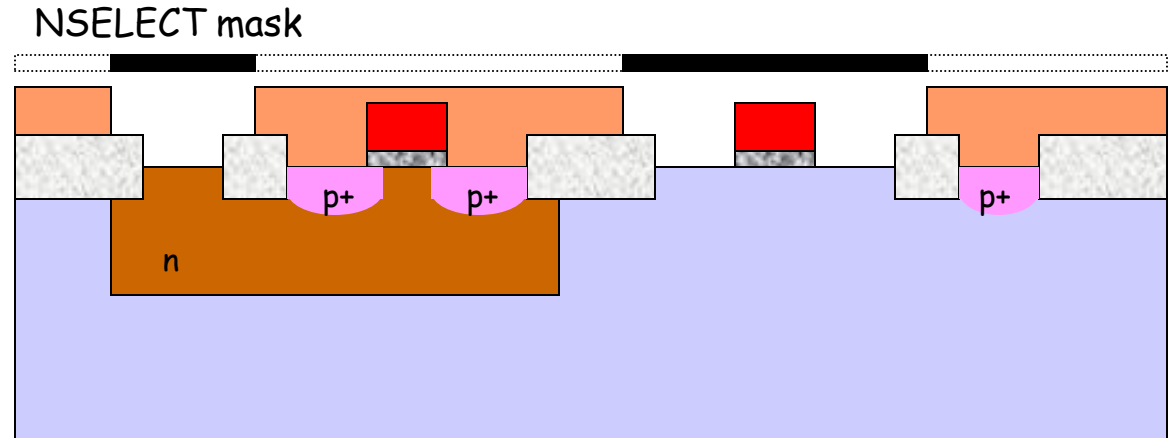
- Cover with photoresist



# LOCOS -step 5

## Form nmos S/D

- Cover with photoresist
- Pattern photoresist
  - \*NSELECT MASK

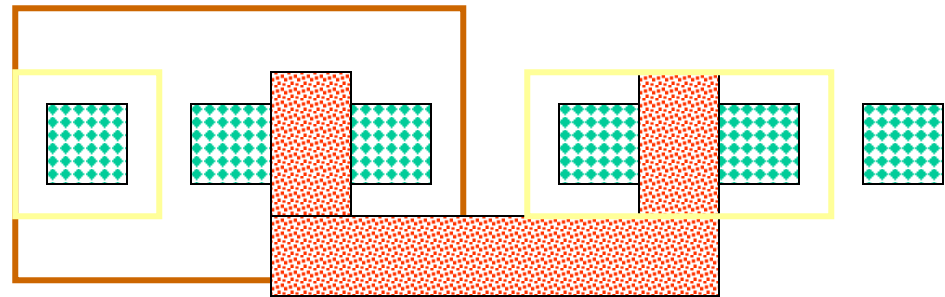
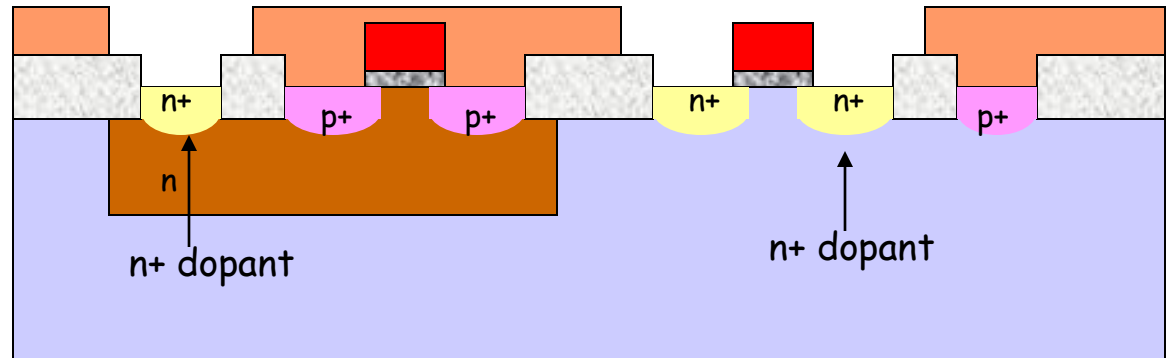


POLY mask

# LOCOS -step 5

## Form nmos S/D

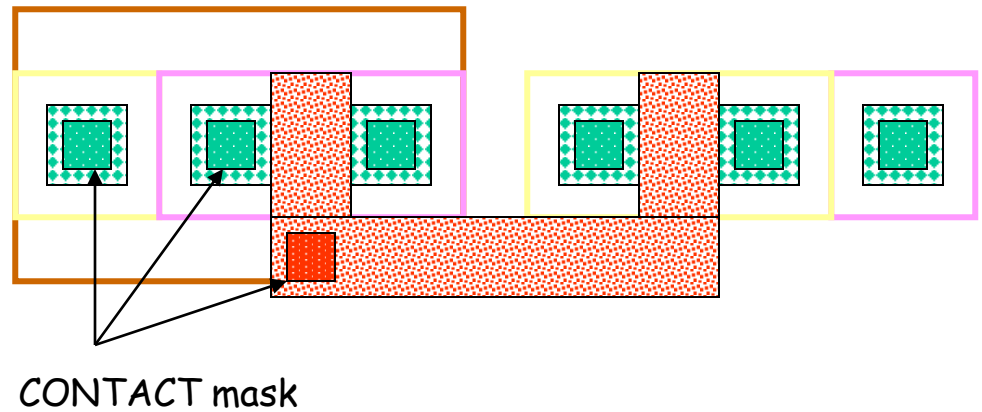
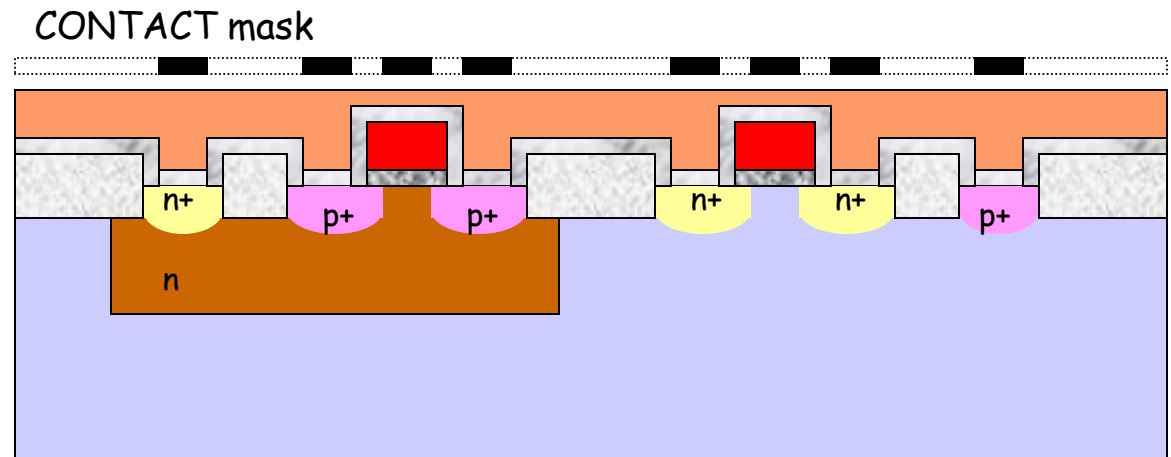
- Cover with photoresist
- Pattern photoresist
  - \*NSELECT MASK
- Implant n-type dopants
- Remove photoresist



# LOCOS -step 6

## Form Contacts

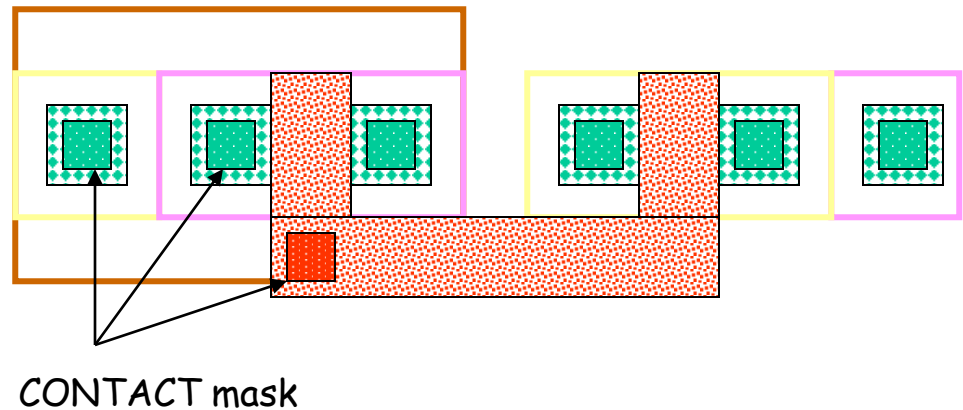
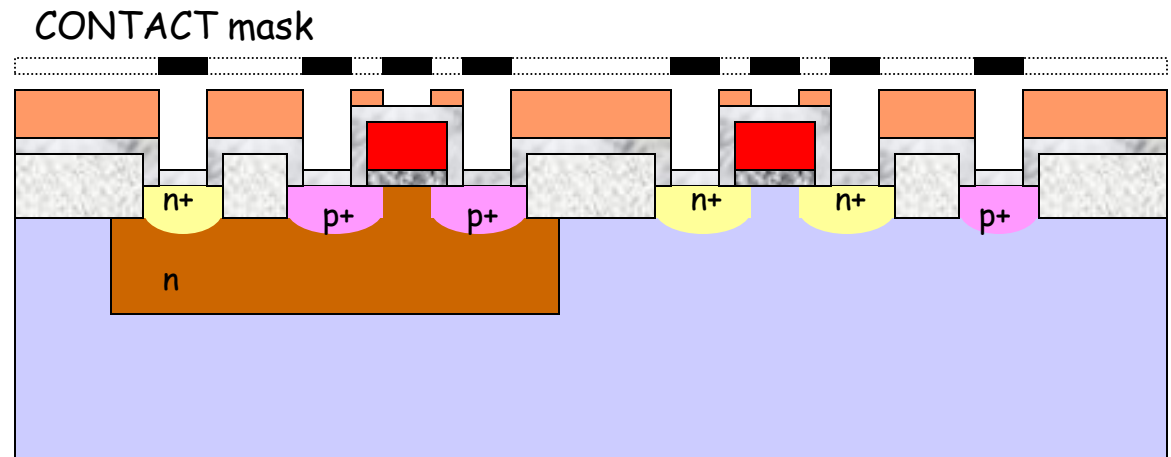
- Deposit oxide
- Deposit photoresist



# LOCOS -step 6

## Form Contacts

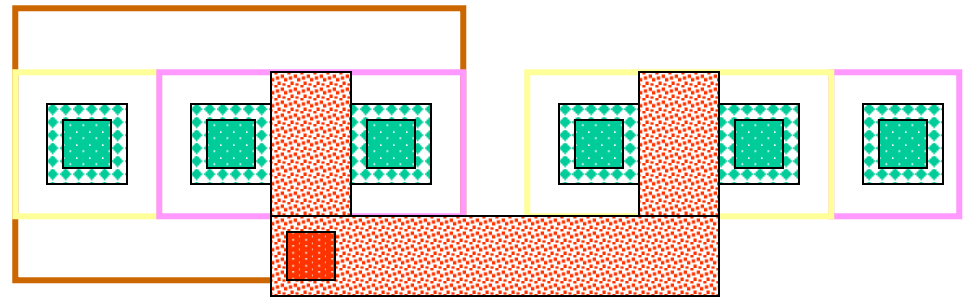
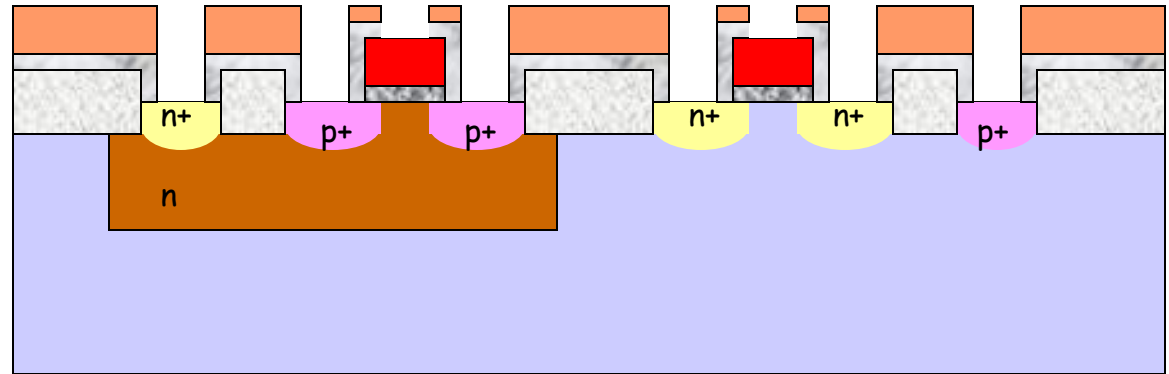
- Deposit oxide
- Deposit photoresist
- Pattern photoresist
  - \*CONTACT Mask
  - One mask for both active and poly contact shown



# LOCOS -step 6

## Form Contacts

- Deposit oxide
- Deposit photoresist
- Pattern photoresist
  - \*CONTACT Mask
  - One mask for both active and poly contact shown
- Etch oxide

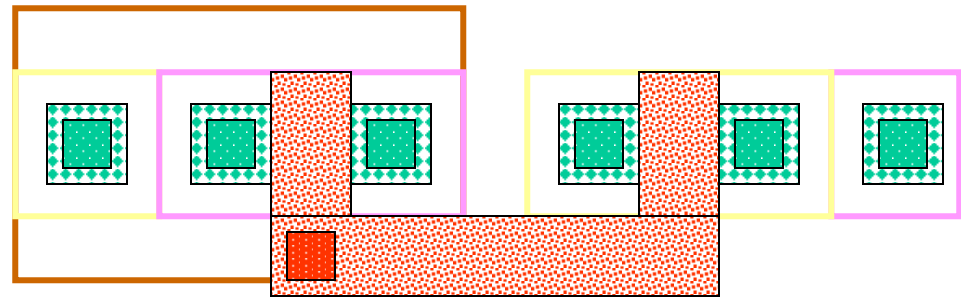
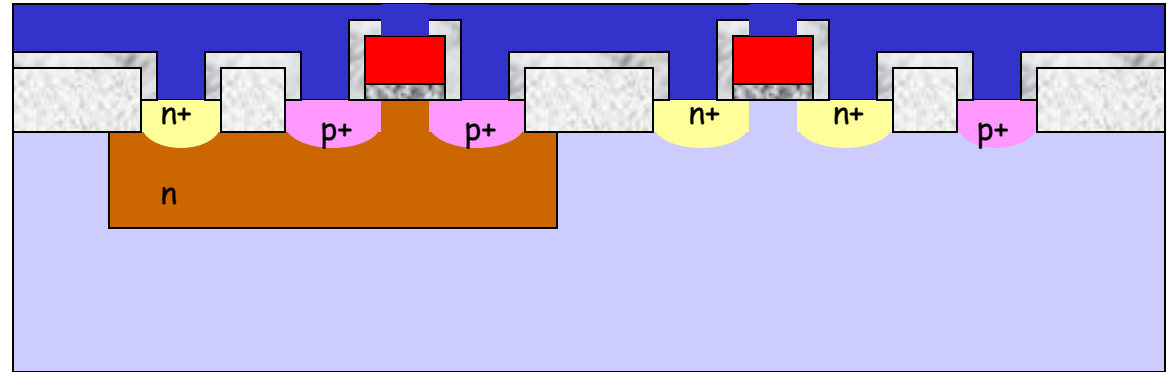




# LOCOS -step 6

## Form Contacts

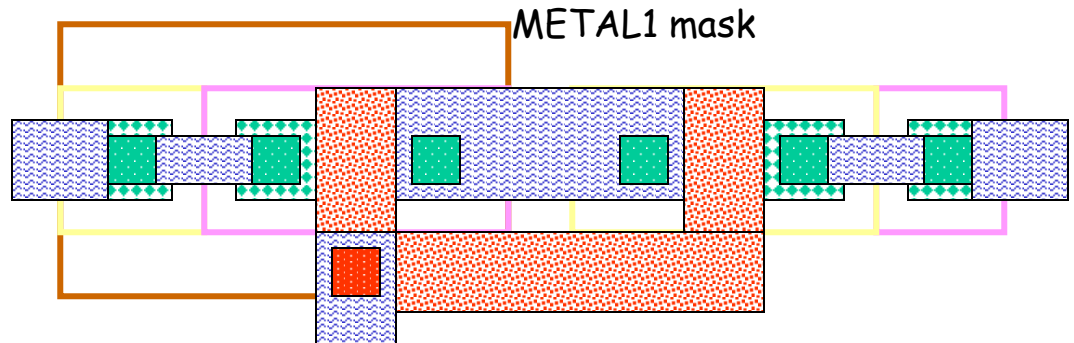
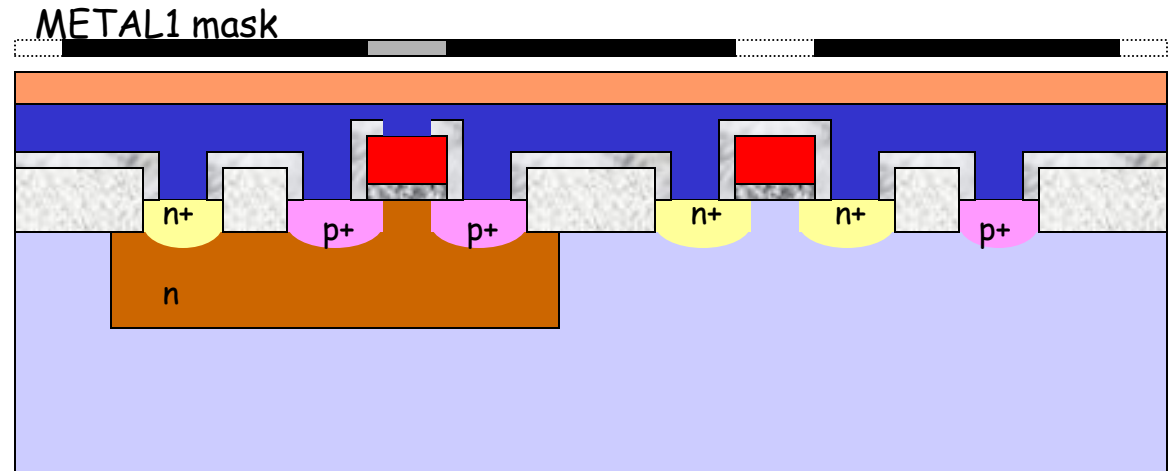
- Deposit oxide
- Deposit photoresist
- Pattern photoresist
  - \*CONTACT Mask
  - One mask for both active and poly contact shown
- Etch oxide
- Remove photoresist
- Deposit metal1
  - immediately after opening contacts so no native oxide grows in contacts
- Planerize
  - make top level



# LOCOS -step 7

## Form Metal 1 Traces

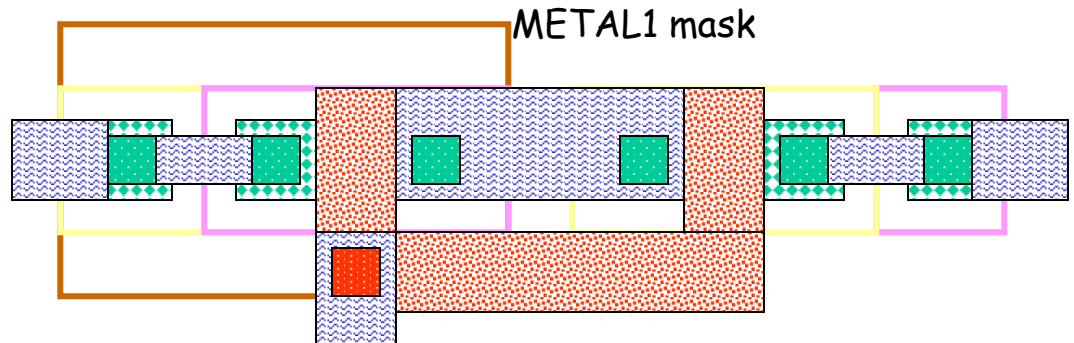
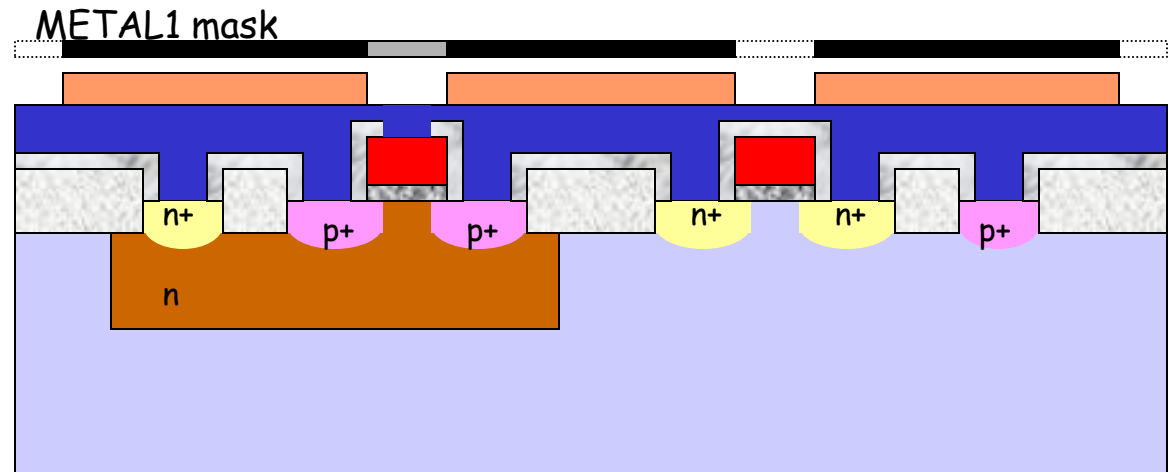
- Deposit photoresist



# LOCOS -step 7

## Form Metal 1 Traces

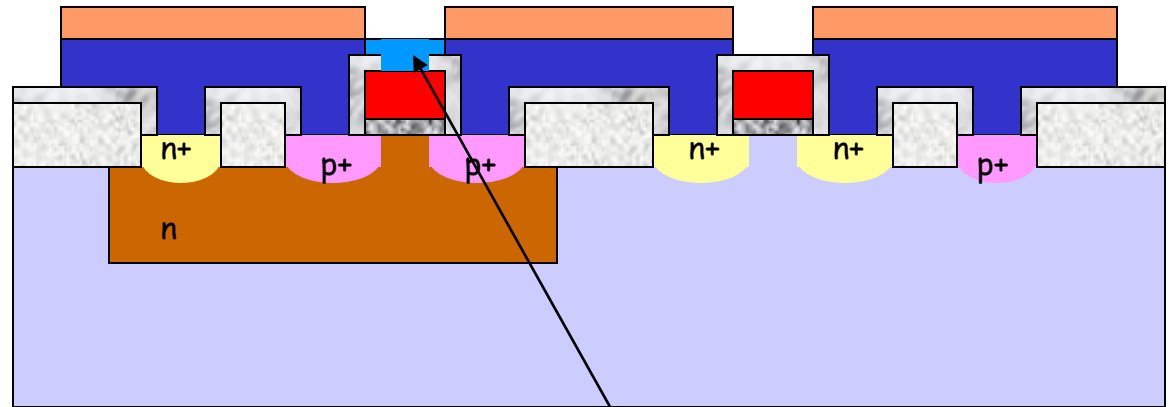
- Deposit photoresist
- Pattern photoresist
  - \*METAL1 Mask



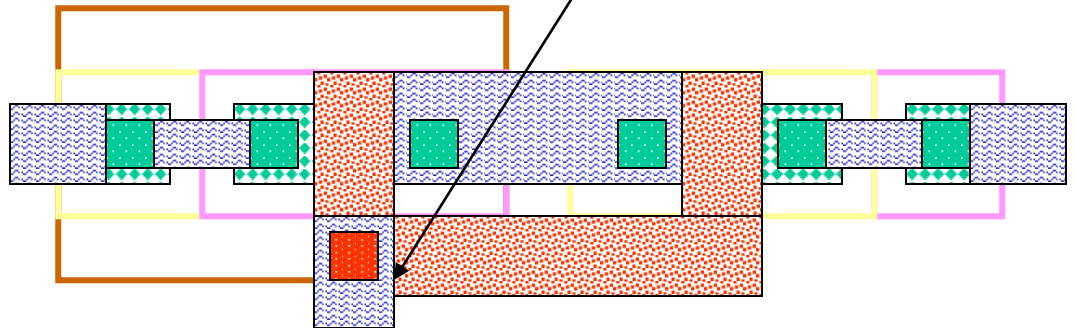
# LOCOS -step 7

## Form Metal 1 Traces

- Deposit photoresist
- Pattern photoresist
  - \*METAL1 Mask
- Etch metal



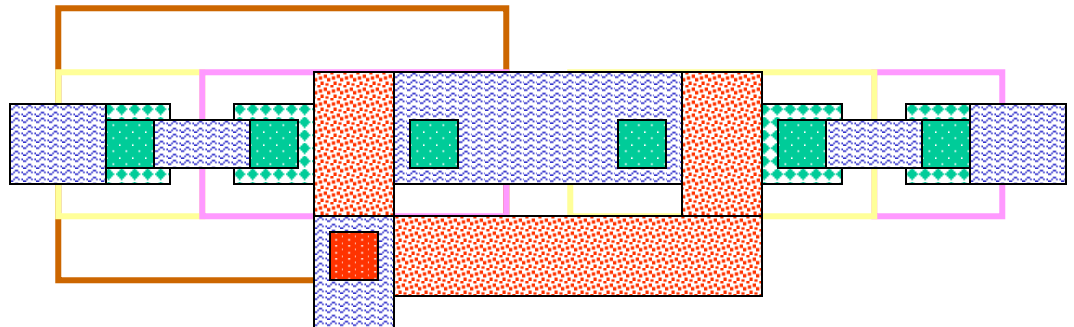
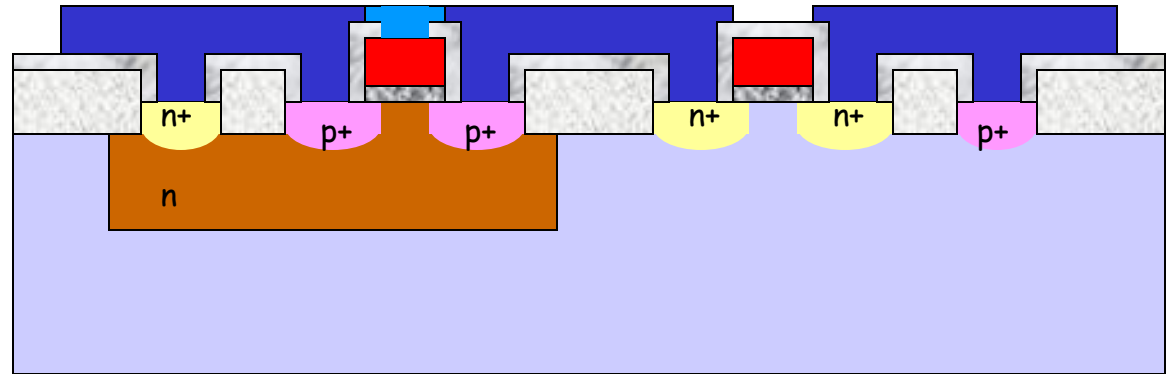
metal over poly outside of cross section



# LOCOS -step 7

## Form Metal 1 Traces

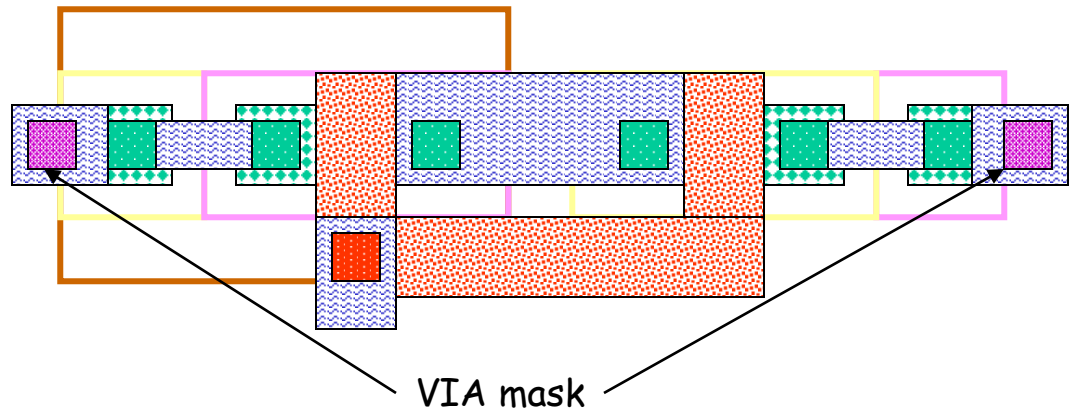
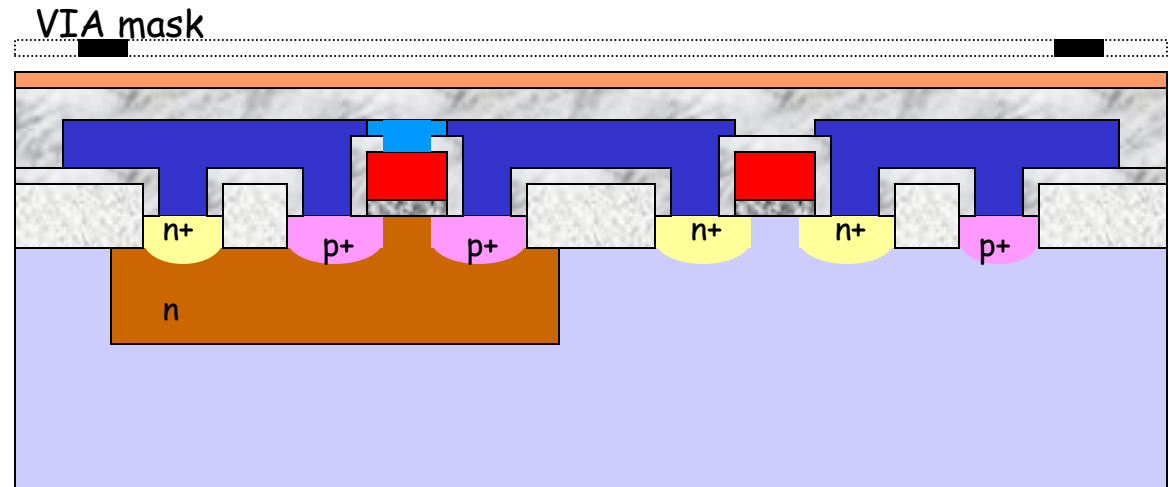
- Deposit photoresist
- Pattern photoresist  
- \*METAL1 Mask
- Etch metal
- Remove photoresist



# LOCOS -step 8

## Form Vias to Metal1

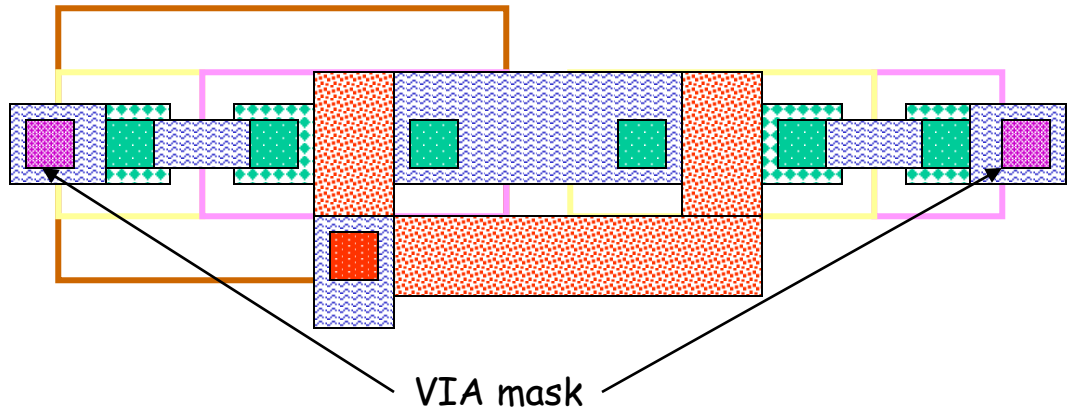
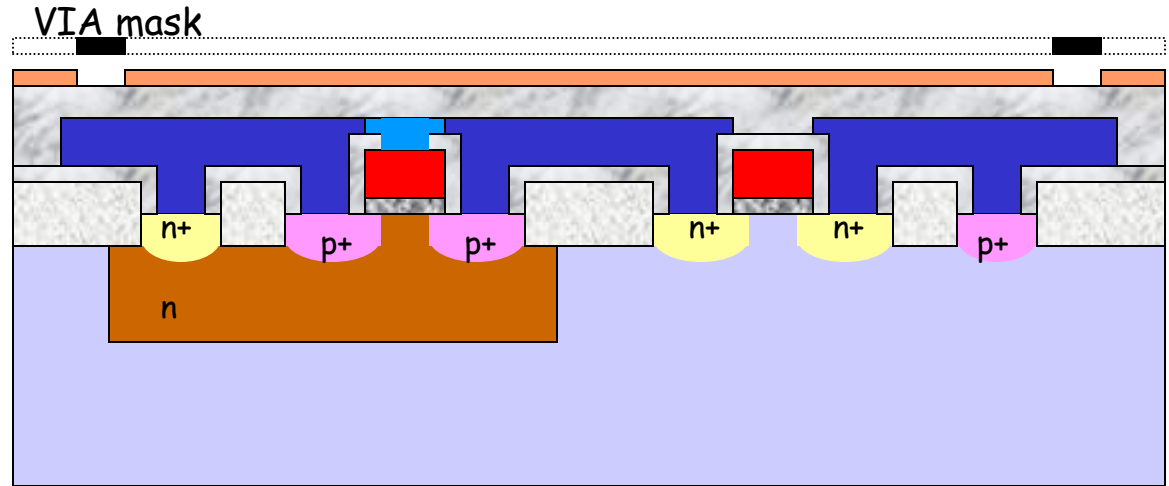
- Deposit oxide
- Planerize oxide
- Deposit photoresist



# LOCOS -step 8

## Form Vias to Metal1

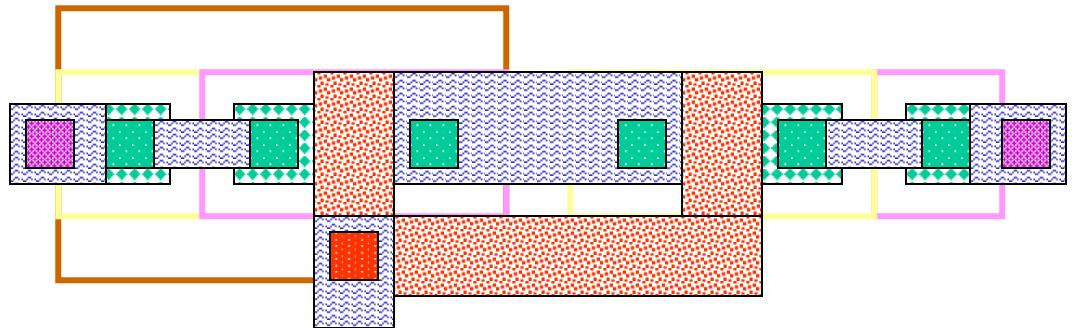
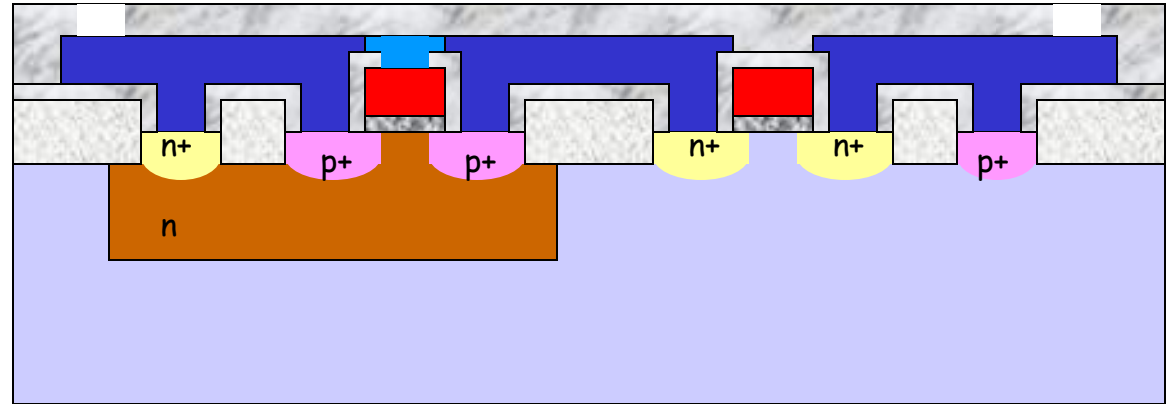
- Deposit oxide
- Planerize
- Deposit photoresist
- Pattern photoresist
  - \*VIA Mask



# LOCOS -step 8

## Form Vias to Metal1

- Deposit oxide
- Planerize
- Deposit photoresist
- Pattern photoresist
  - \*VIA Mask
- Etch oxide
- Remove photoresist

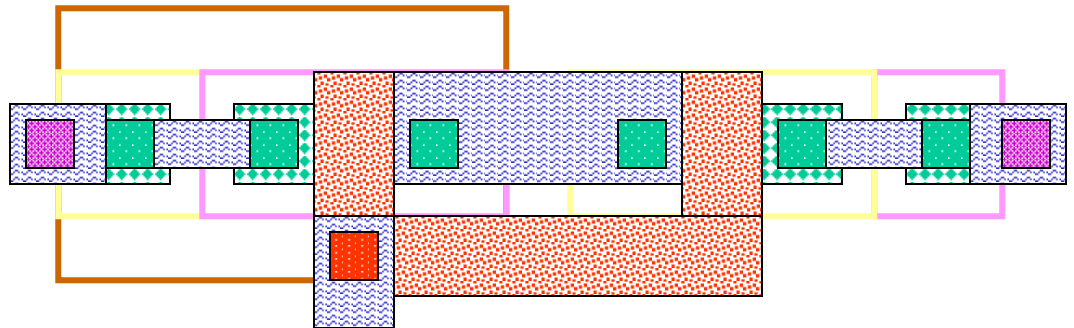
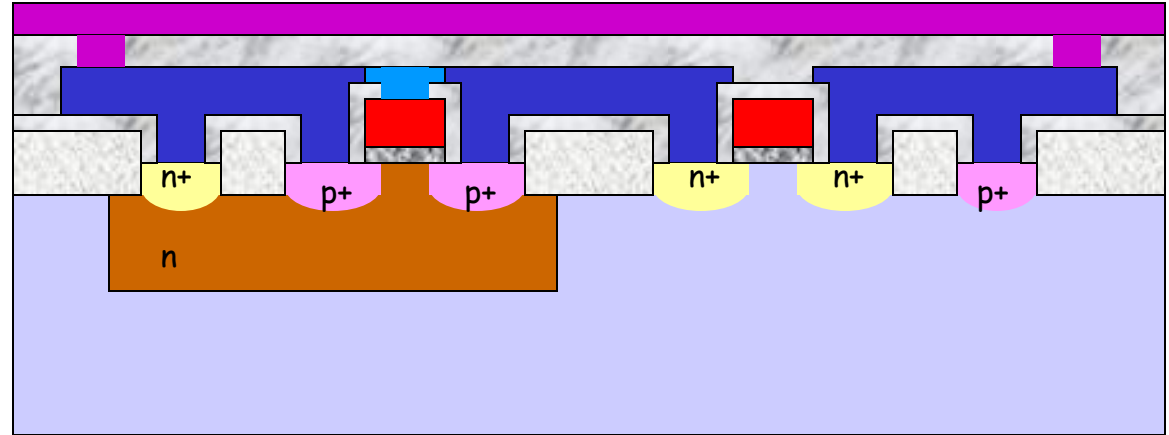




# LOCOS -step 8

## Form Vias to Metal1

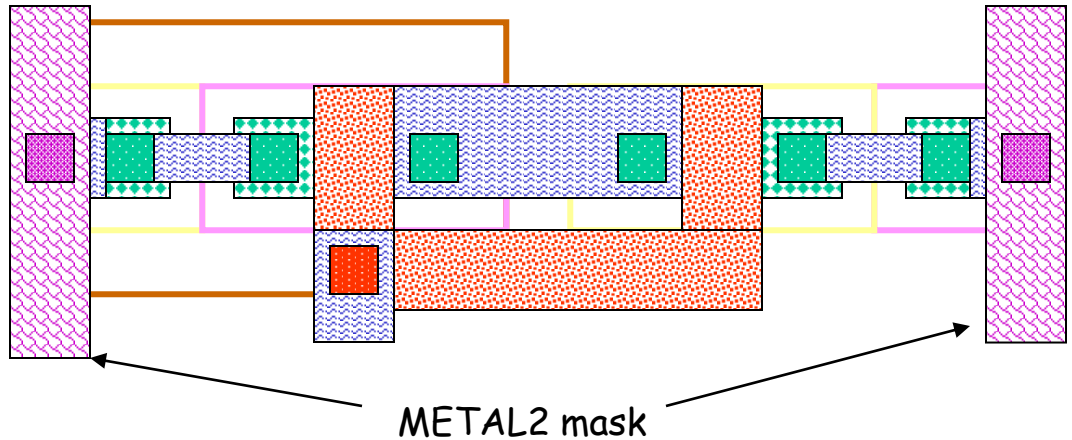
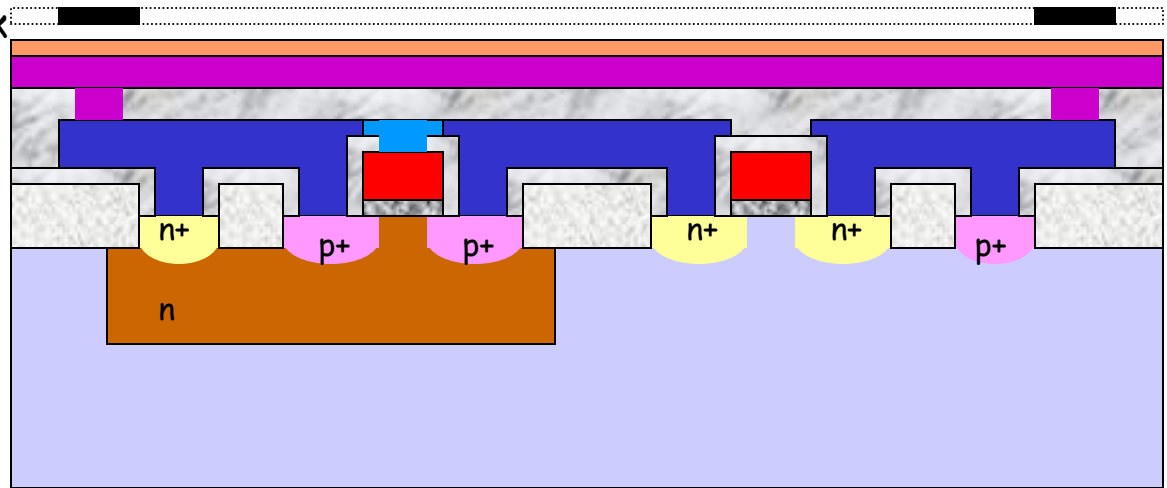
- Deposit oxide
- Planerize
- Deposit photoresist
- Pattern photoresist
  - \*VIA Mask
- Etch oxide
- Remove photoresist
- Deposit Metal2



# LOCOS -step 9

METAL2 mask  
Form Metal2 Traces

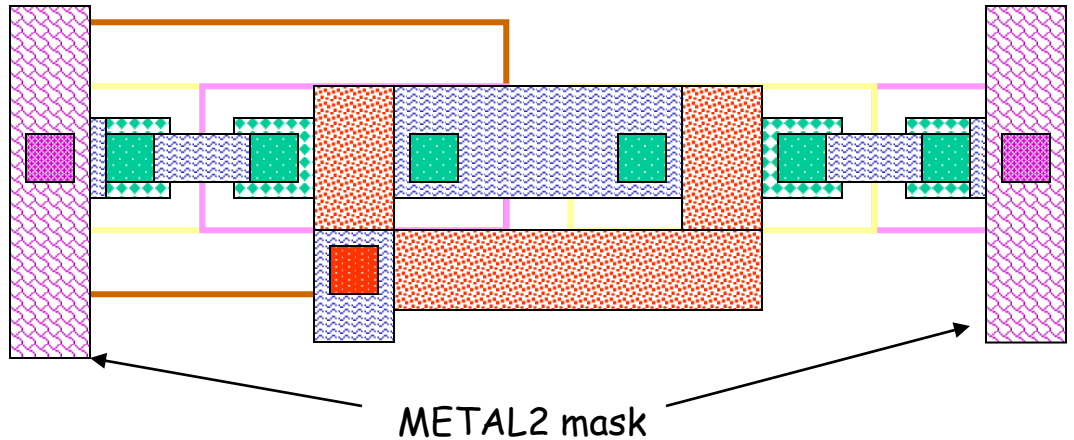
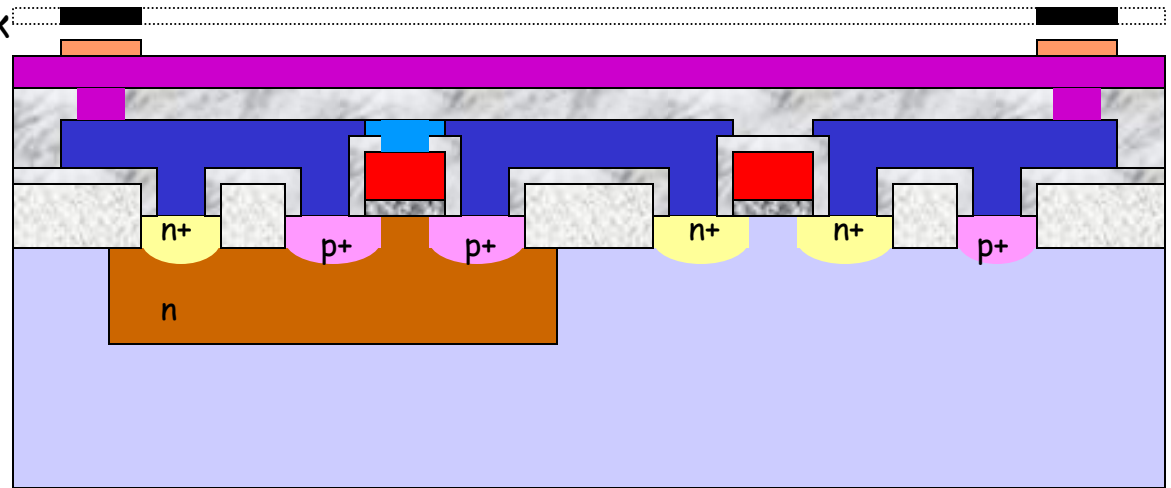
- Deposit photoresist



# LOCOS -step 9

METAL2 mask  
Form Metal2 Traces

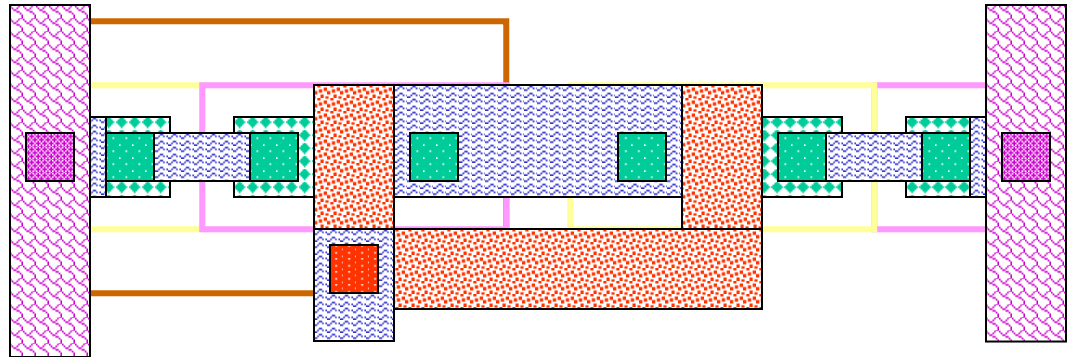
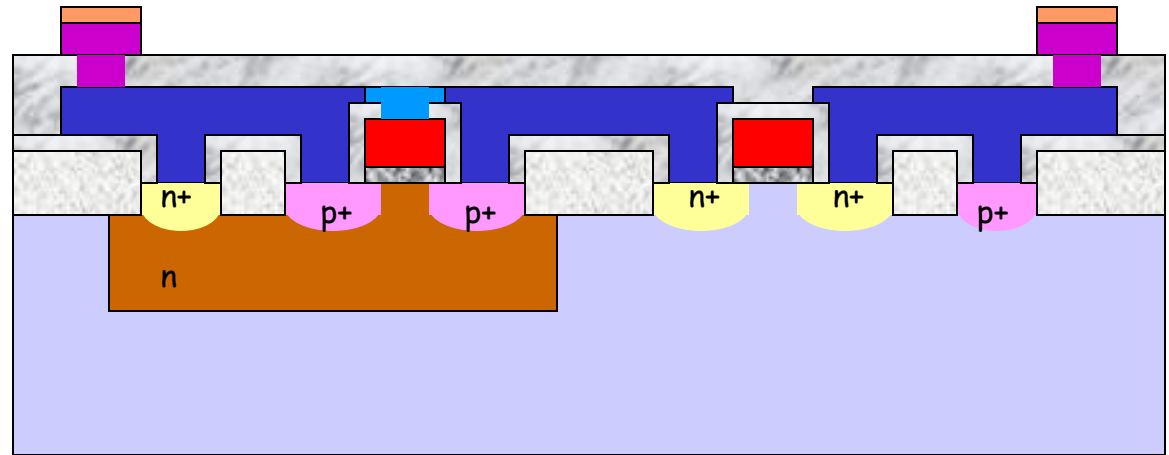
- Deposit photoresist
- Pattern photoresist  
- \*METAL2 Mask



# LOCOS -step 9

## Form Metal2 Traces

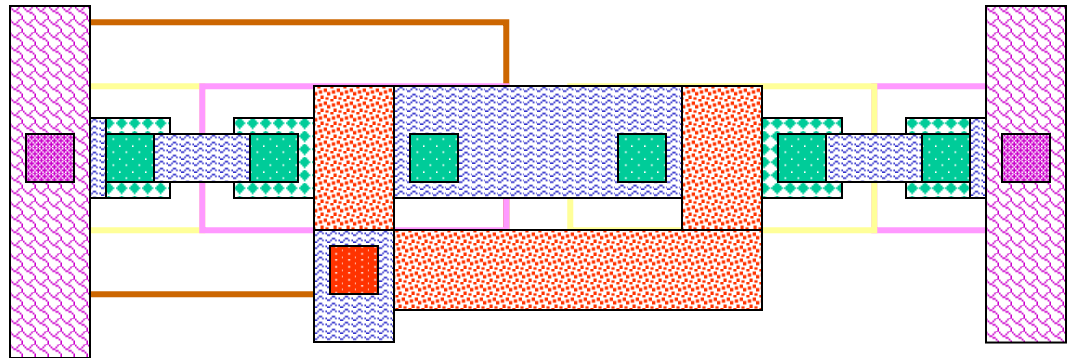
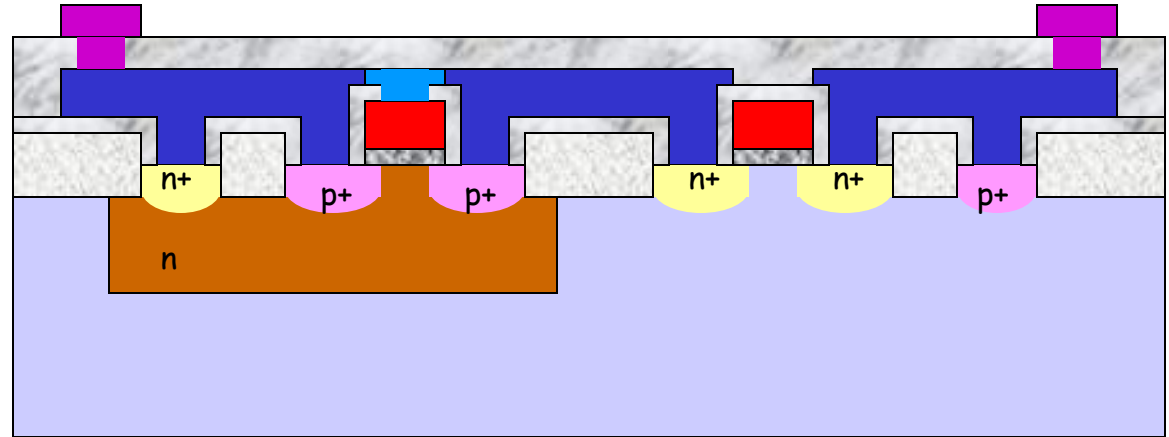
- Deposit photoresist
- Pattern photoresist  
- \*METAL2 Mask
- Etch metal



# LOCOS -step 9

## Form Metal2 Traces

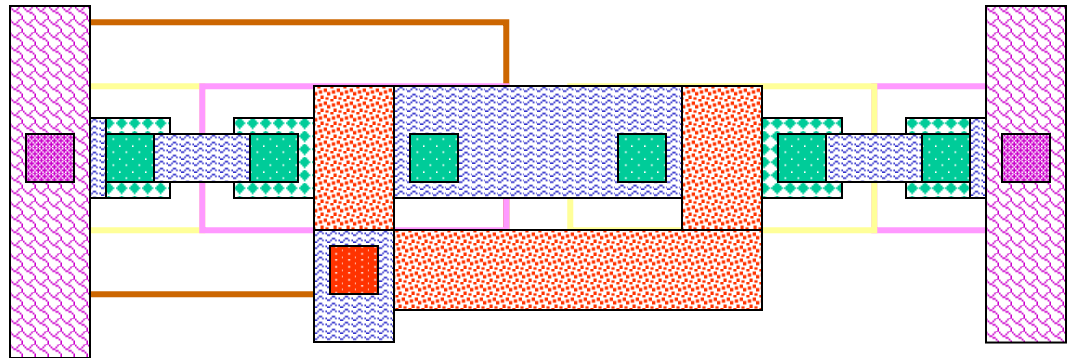
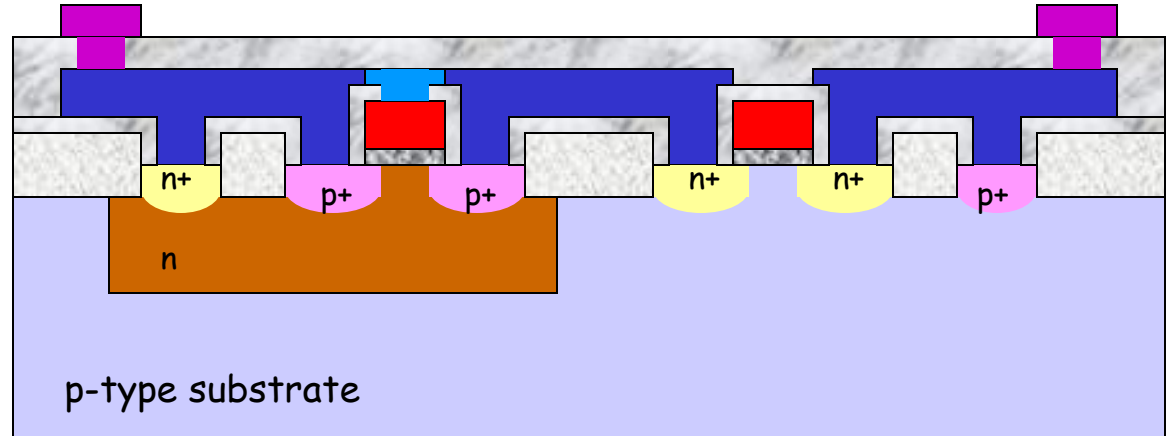
- Deposit photoresist
- Pattern photoresist  
- \*METAL2 Mask
- Etch metal
- Remove photoresist



# LOCOS -step 10+

## Form Additional Traces

- Deposit oxide
- Deposit photoresist
- Pattern photoresist
- Etch oxide
- Deposit metal
- Deposit photoresist
- Pattern photoresist
- Etch metal
- Repeat for each additional metal



# Simplifications from complete process

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- skipped several substrate doping steps
  - channel implant to adjust threshold voltages
  - surface implant to increase breakdown voltage
- no LDD, lightly-doped drain
- no deposition of contact interface materials
- metal patterning simplified
  - more complex "lift-off" process often used
- no overglass (thick top dielectric) layer
- no bonding pad layer
- simplified use of dark/clear field masks and positive/negative photoresist