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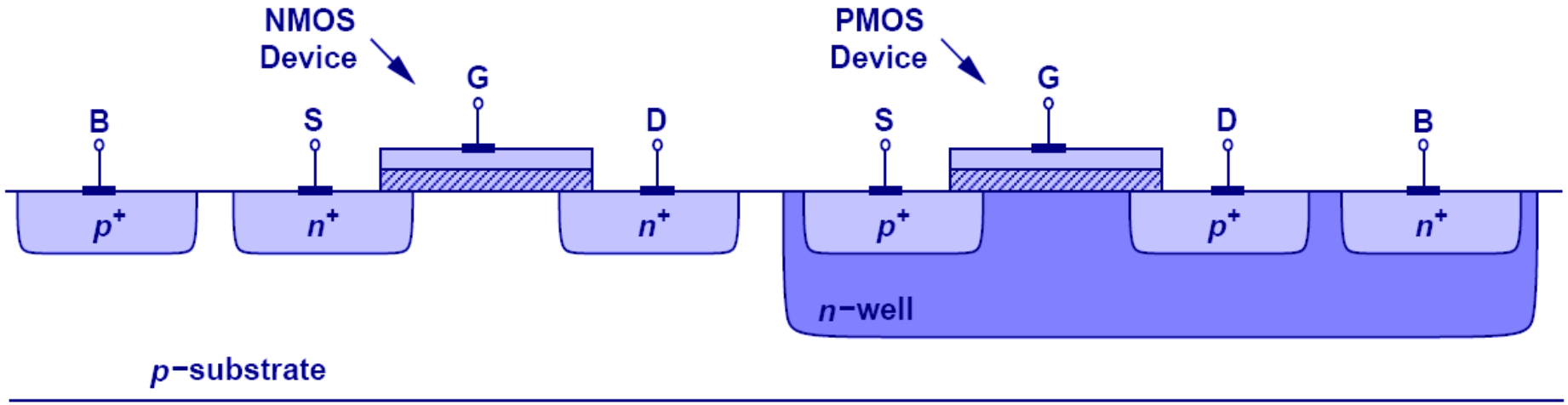
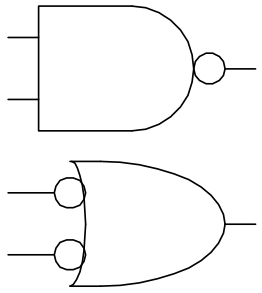
CMOS Technology

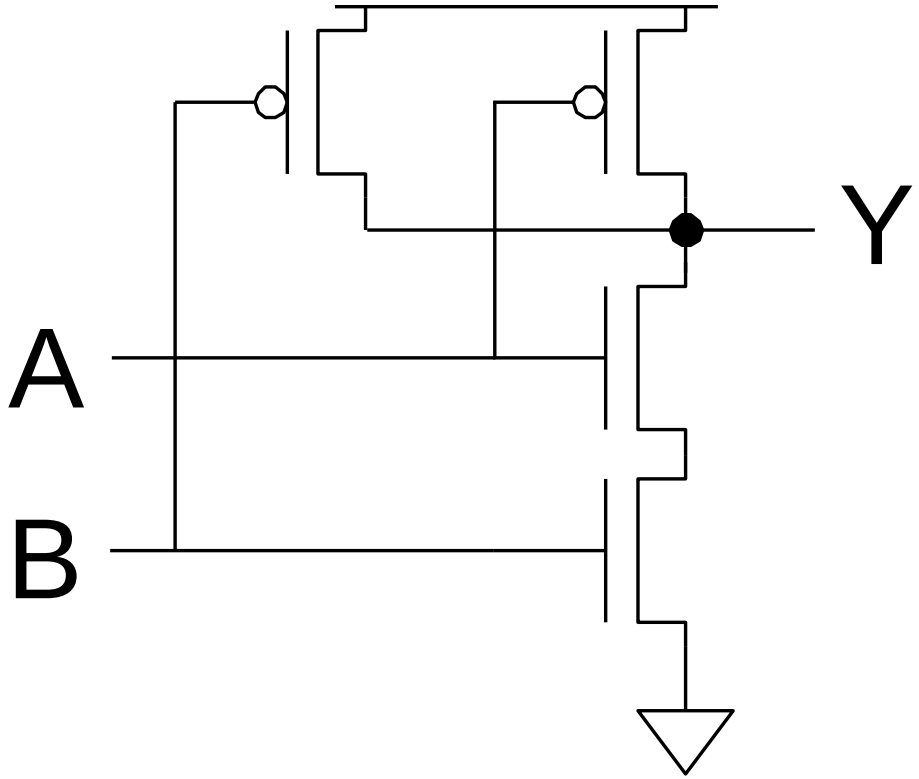


- It possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.
- It is known as CMOS, or “Complementary MOS”.

CMOS **NAND** Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

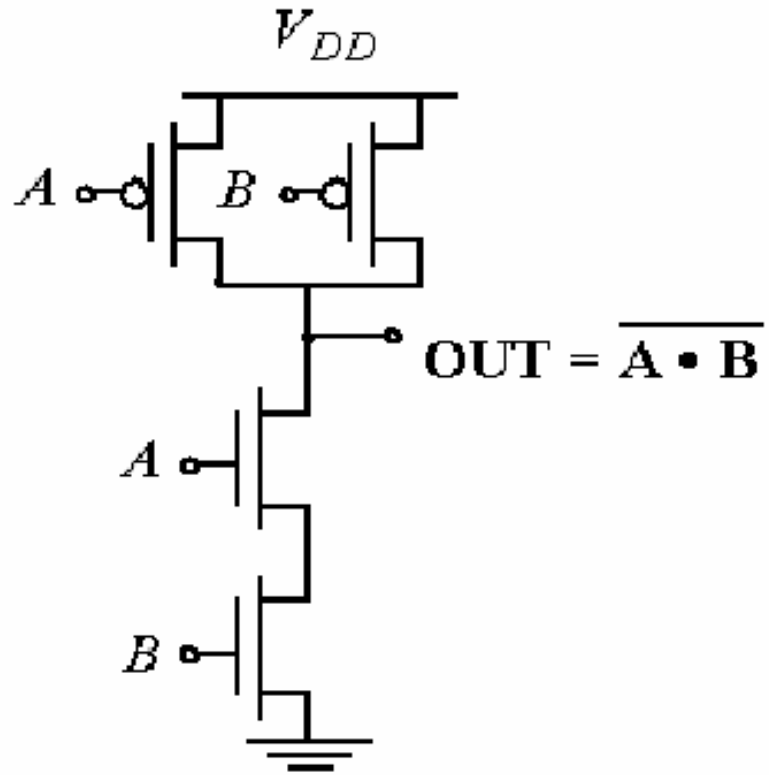




Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



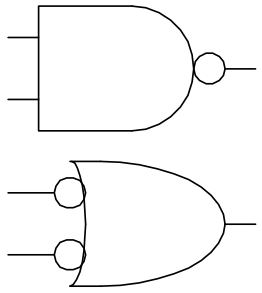
PDN: G = A B $\Rightarrow$ Conduction to GND

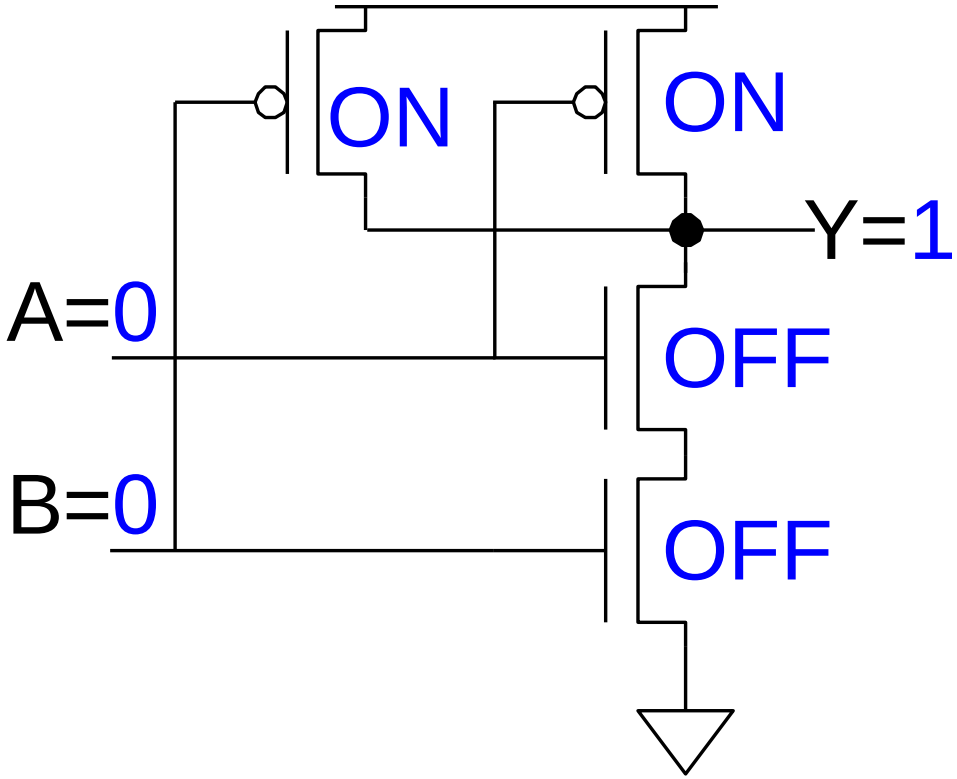
PUN: F= $\overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}

$$\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$$

CMOS **NAND** Gate

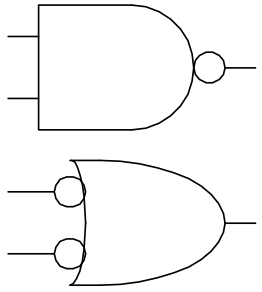
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

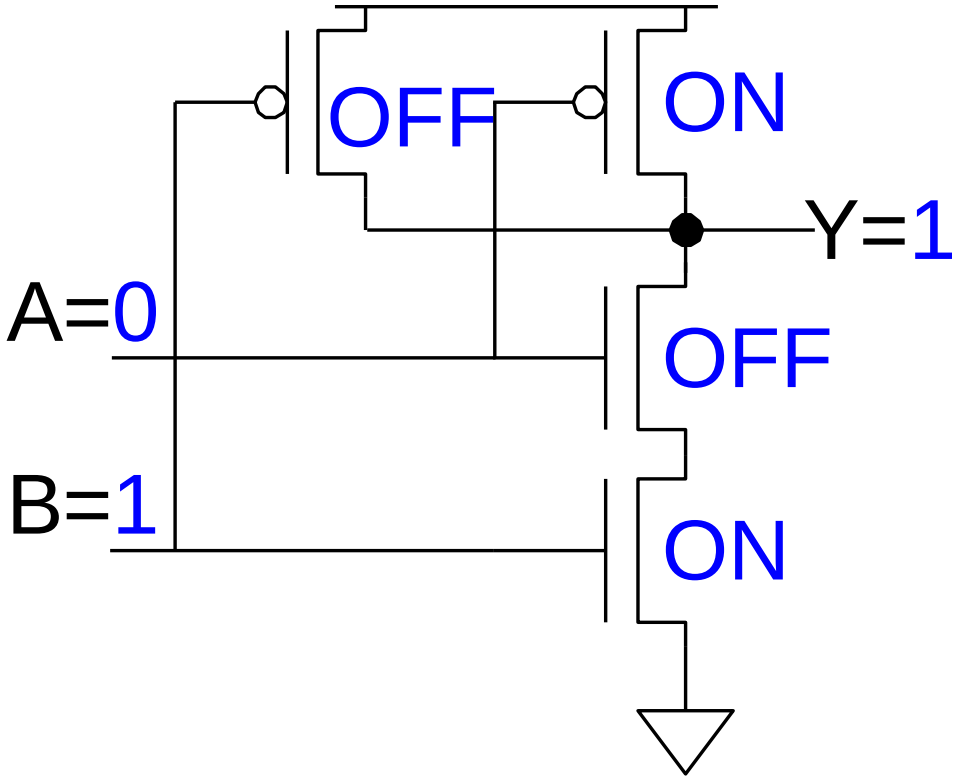




CMOS **NAND** Gate

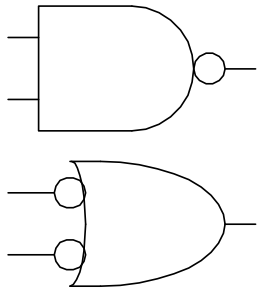
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

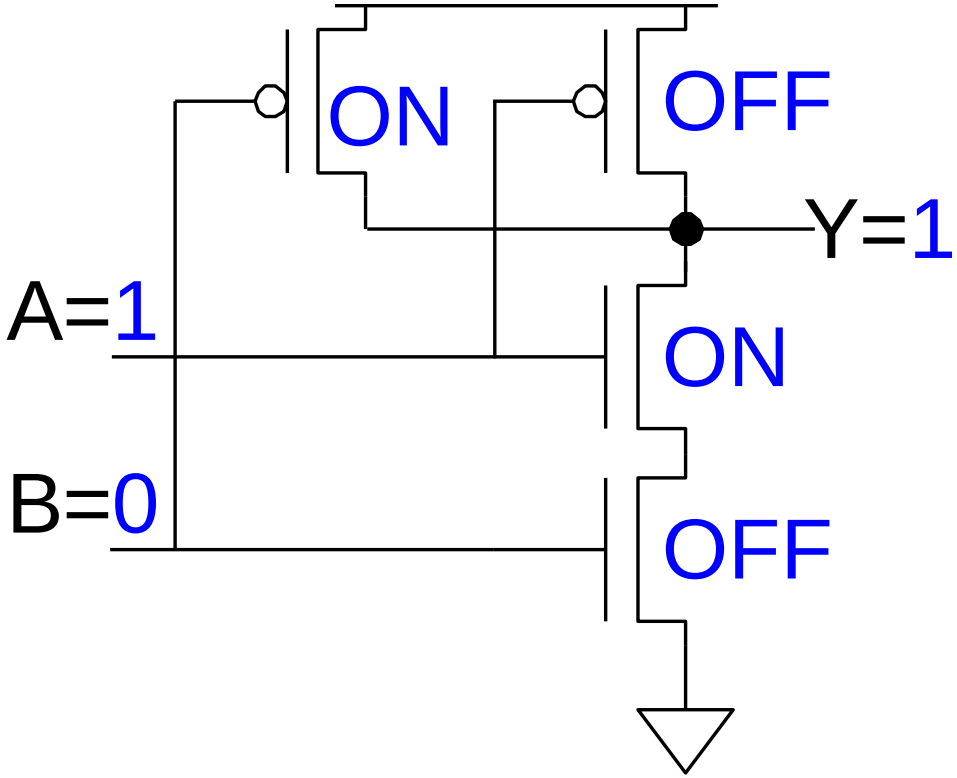




CMOS **NAND** Gate

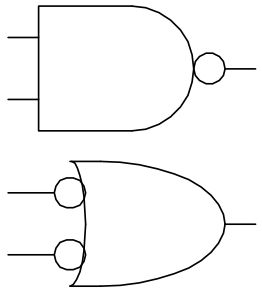
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

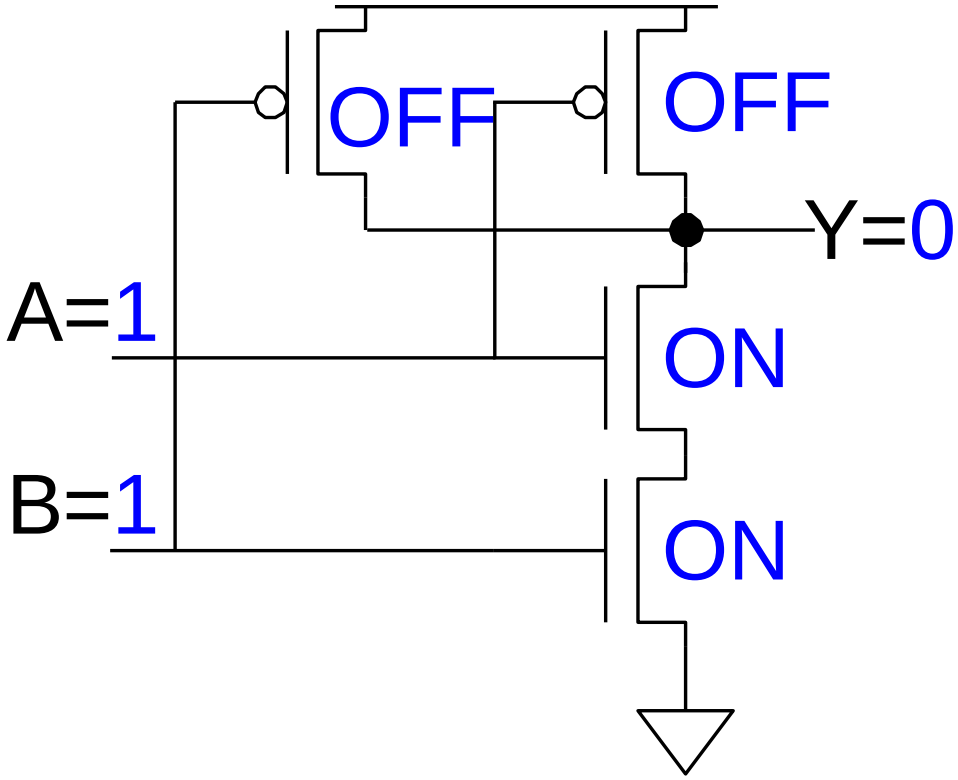




CMOS **NAND** Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**





NAND2

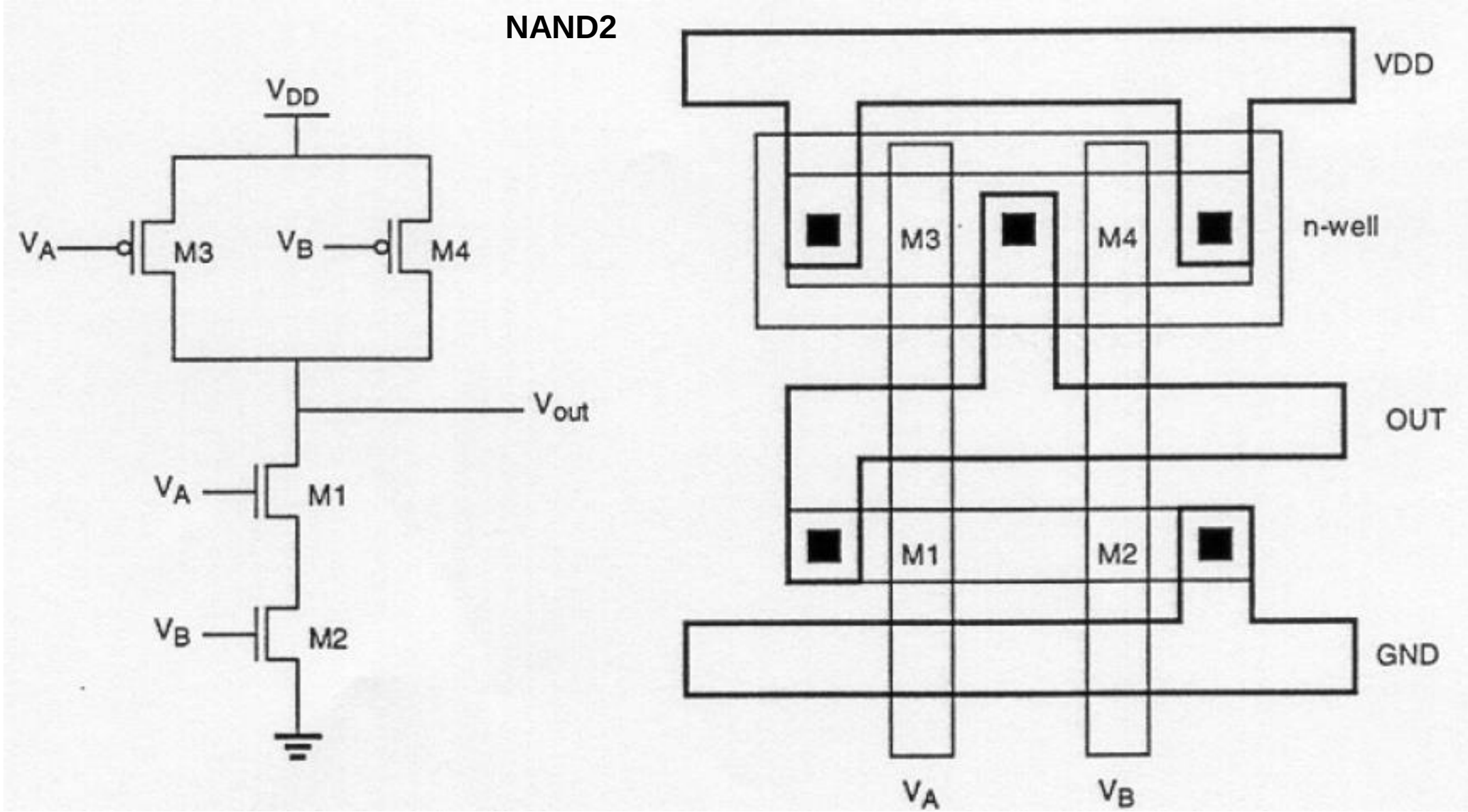


Figura 3.7: Forma mastilor- mostra ale unor porti CMOS NOR2 si NAND2

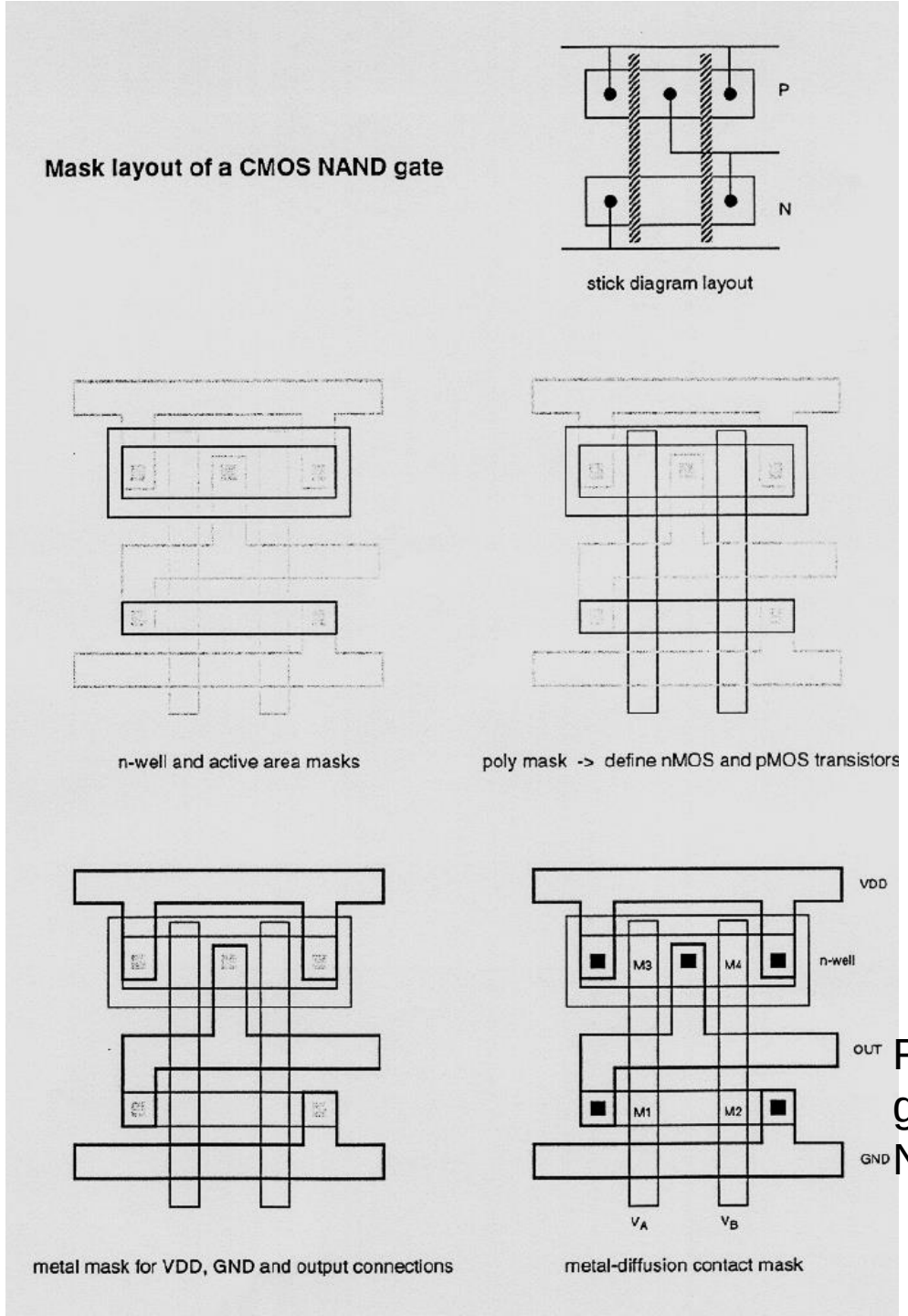
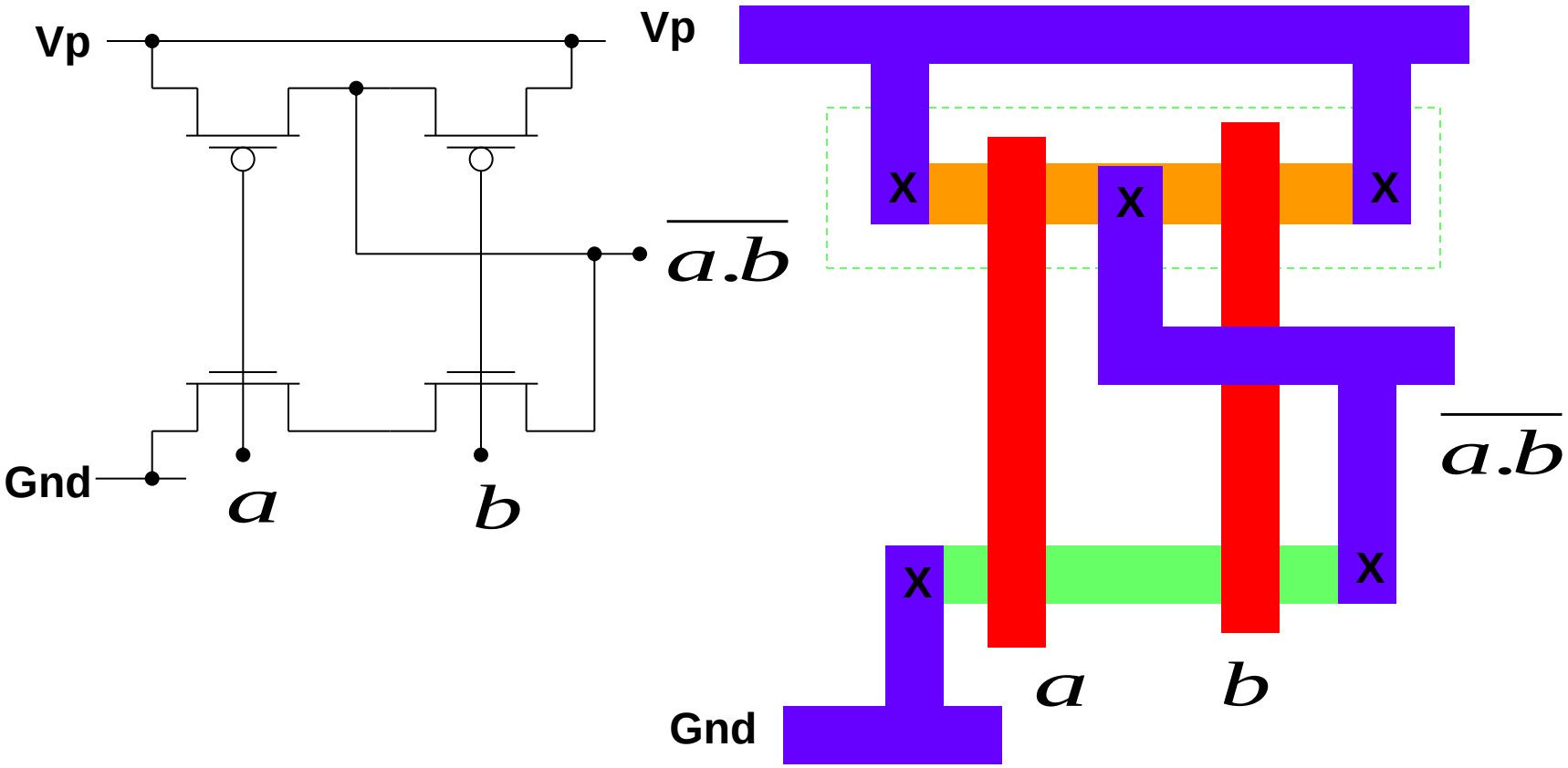
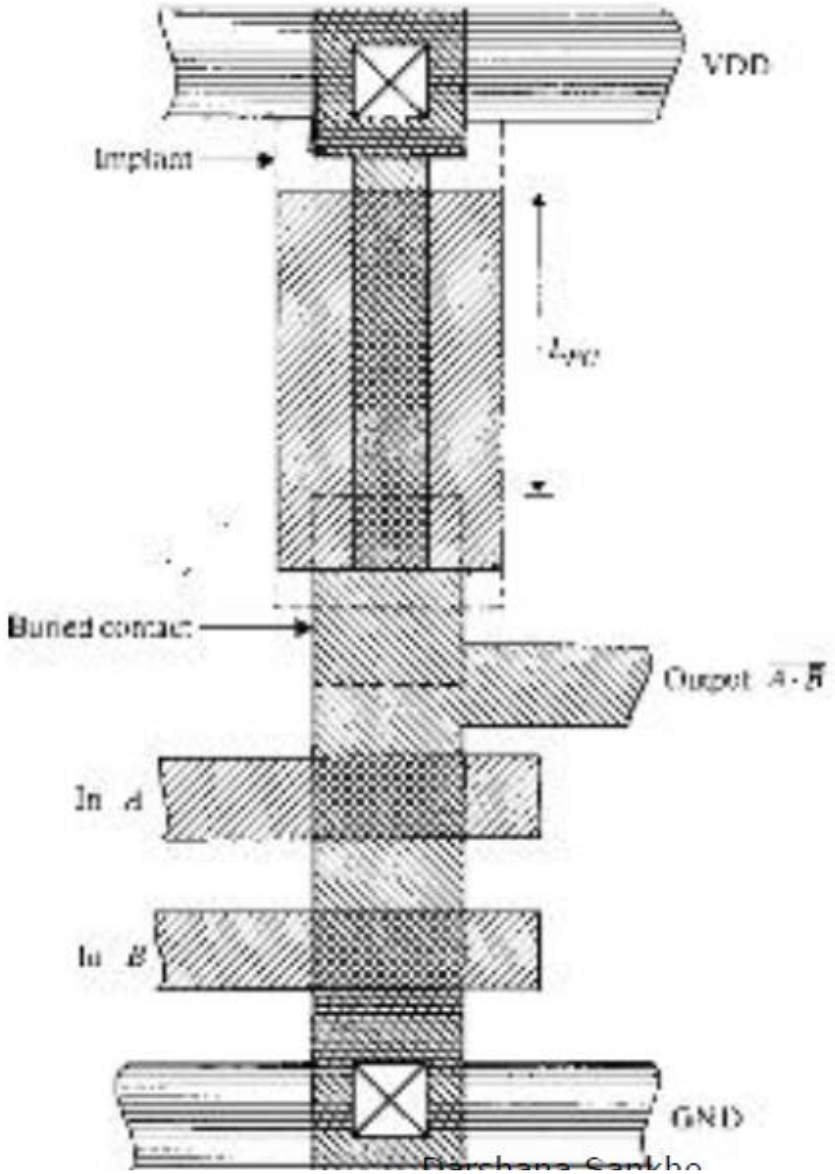


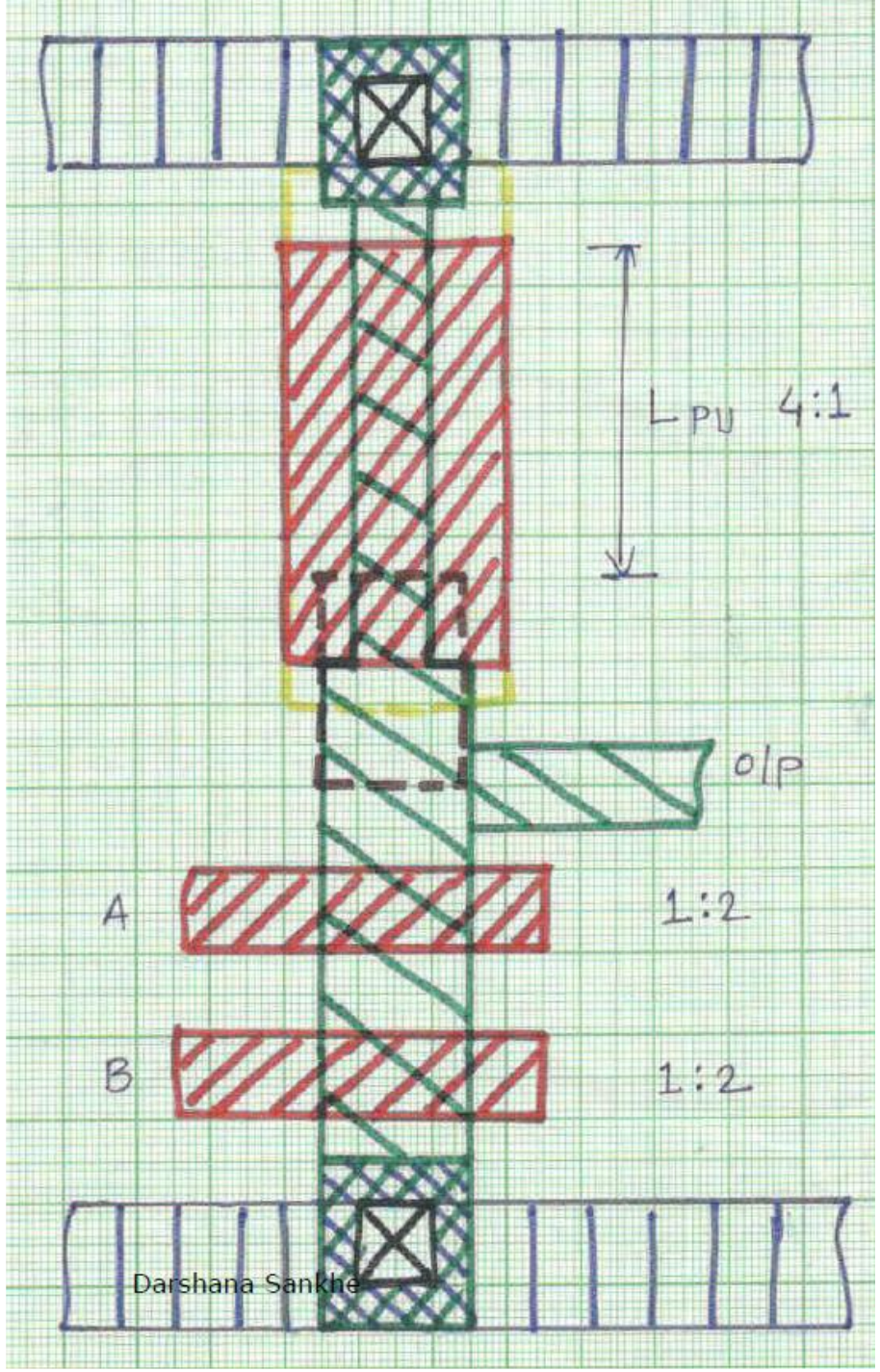
Figura 3.9: Pasii principali necesari pentru generareai mastlor unei porti CMOS NAND2

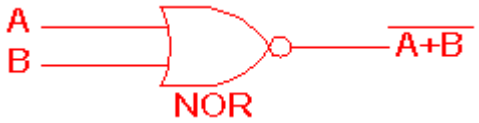
NAND2 Layout



NMOS NAND

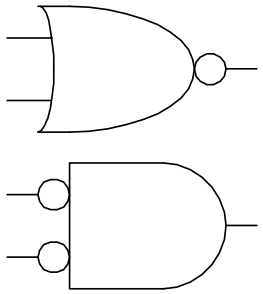

VDD
Implant
Buried contact
Output A·B
In A
In B
GND

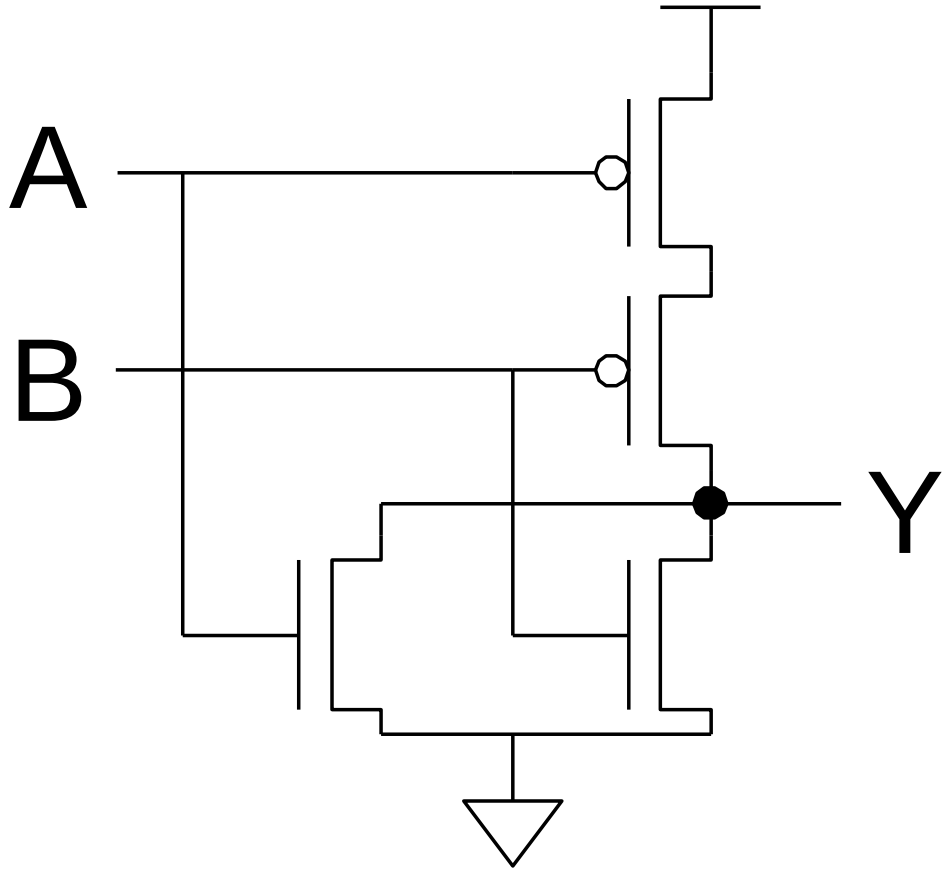

L PU 4:1
o/p
A
1:2
B
1:2
Darshana Sankhe

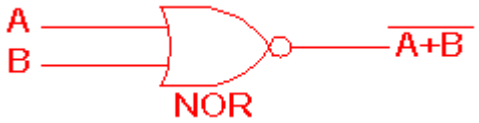


CMOS **NOR** Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



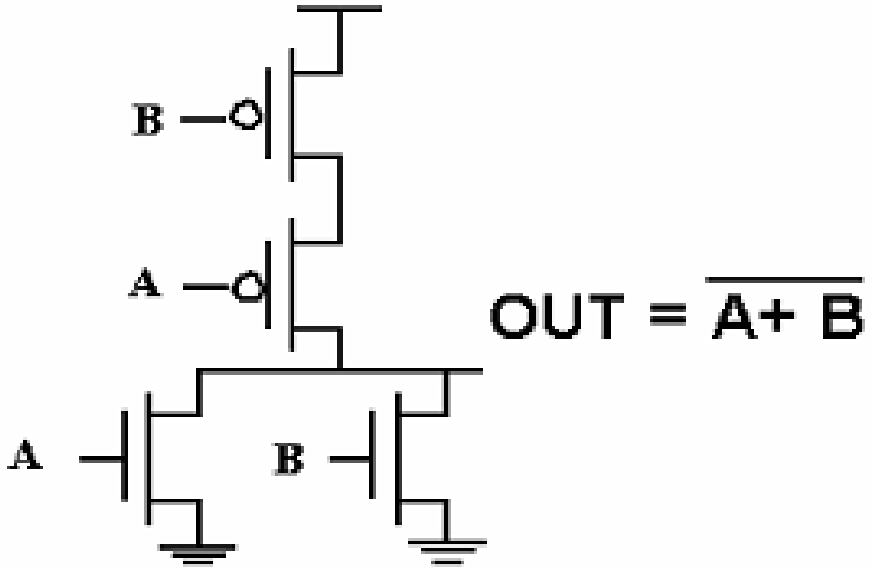


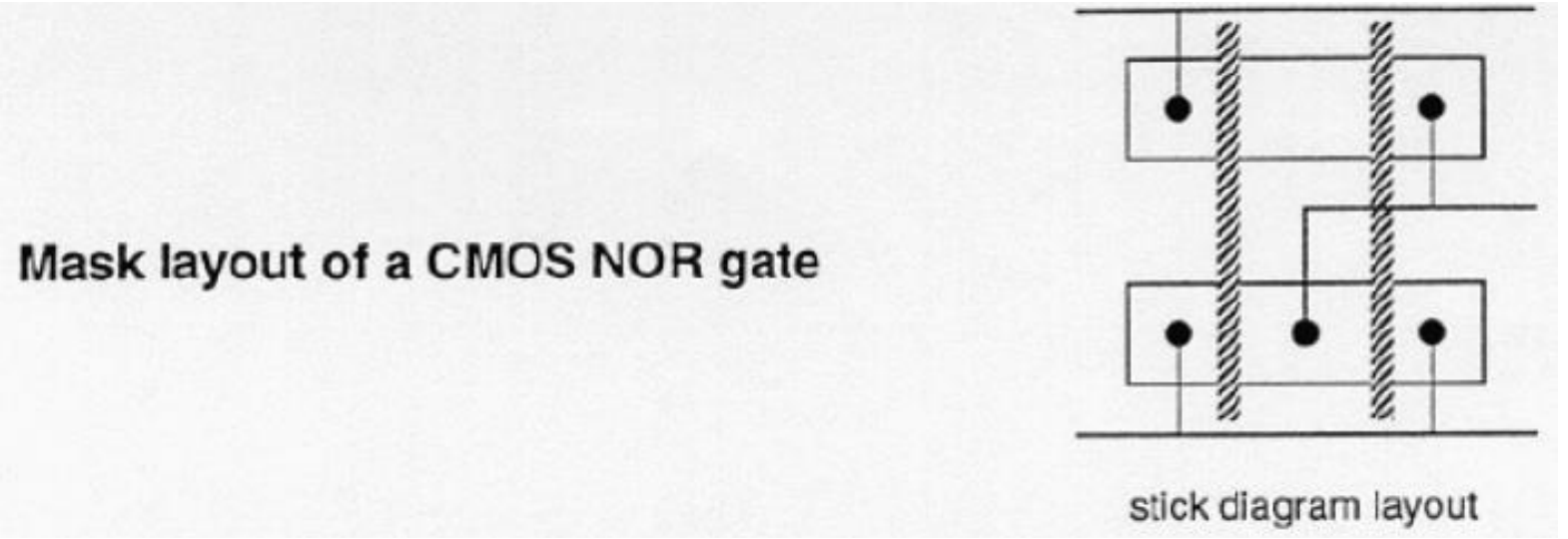


Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate





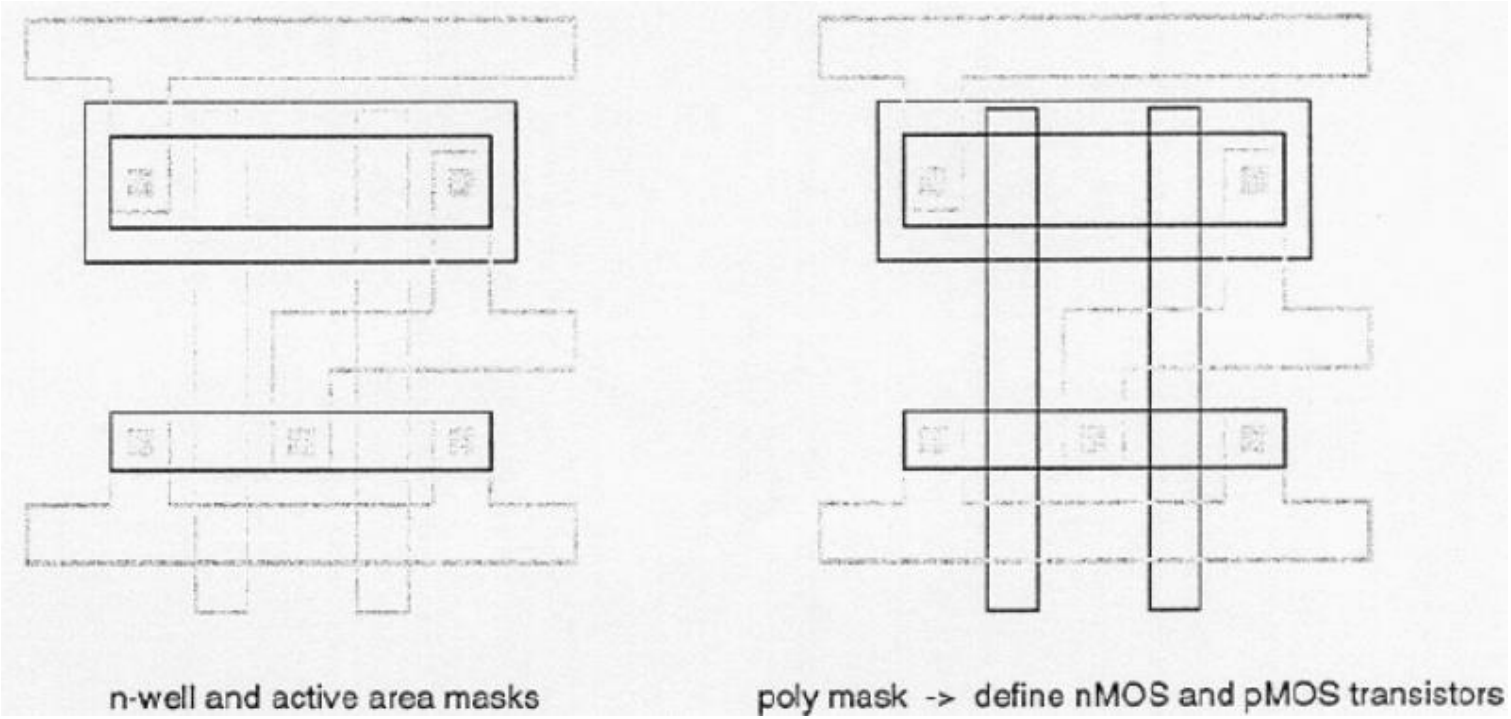


Figura 3.8: Pasii principali necesari pentru generarea mastilor unei porti CMOS NOR2

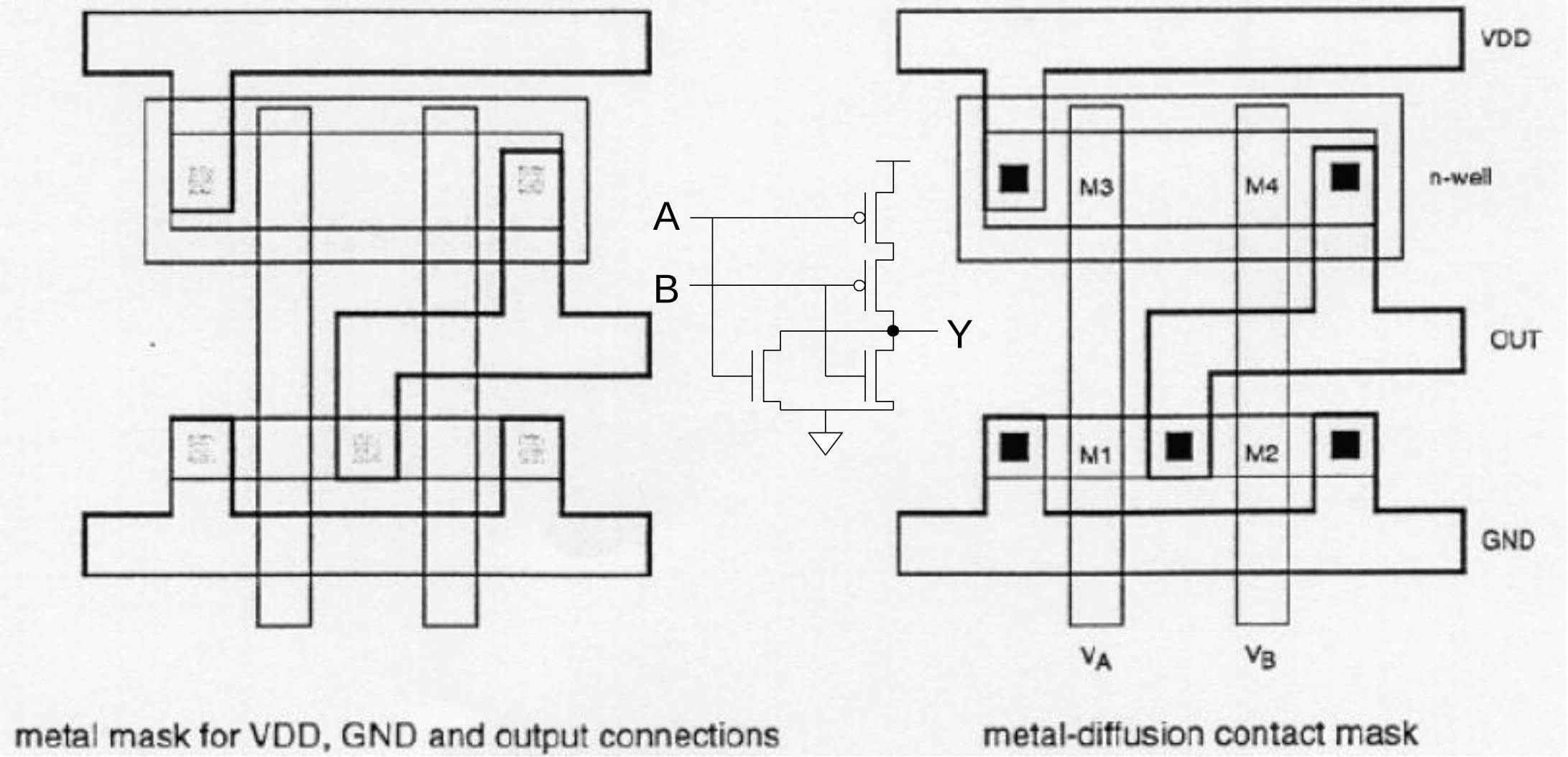
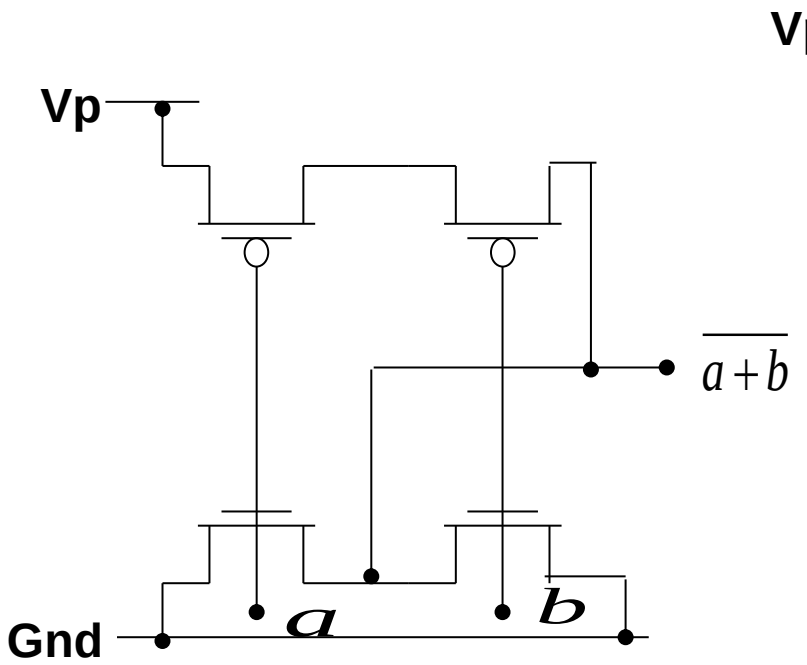
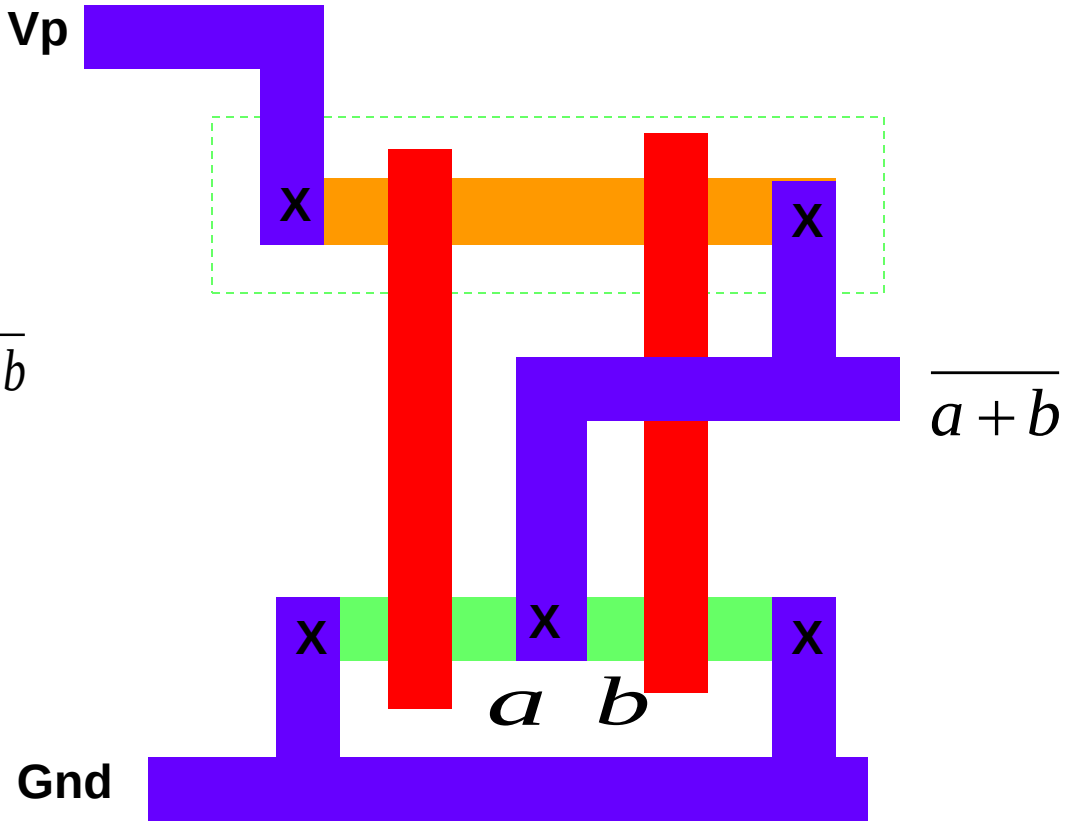


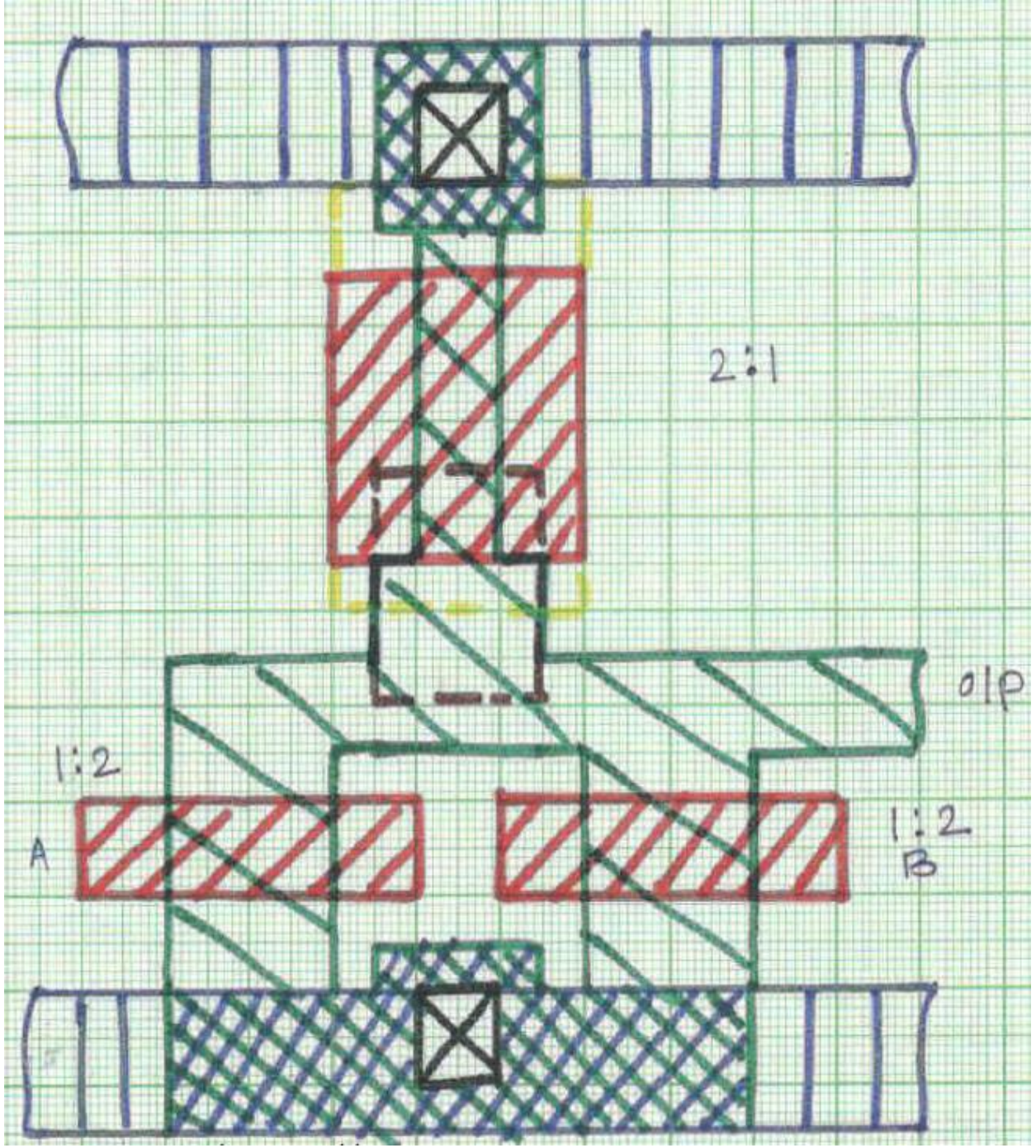
Figura 3.8: Pasii principali necesari pentru generarea mastilor unei porti CMOS NOR2

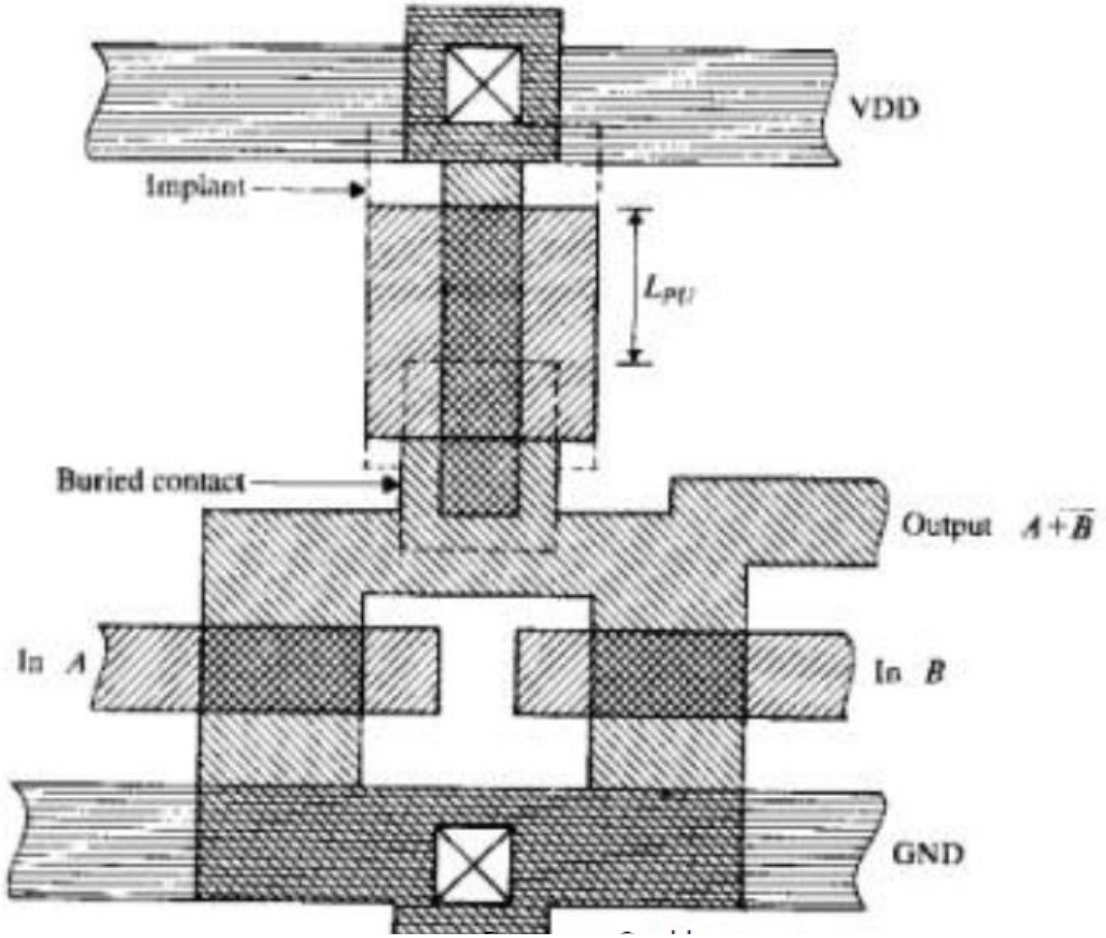
NOR2 Layout





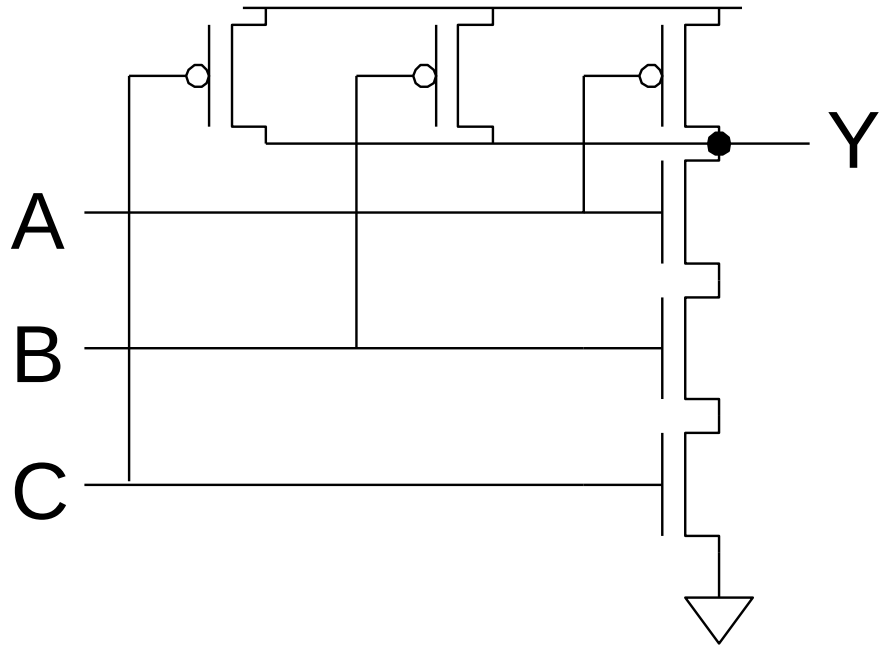
NMOS NOR


2:1
1:2
A
1:2
B
O/P


VDD
Implant
L_{pu}
Buried contact
Output $A+\overline{B}$
In A
In B
GND

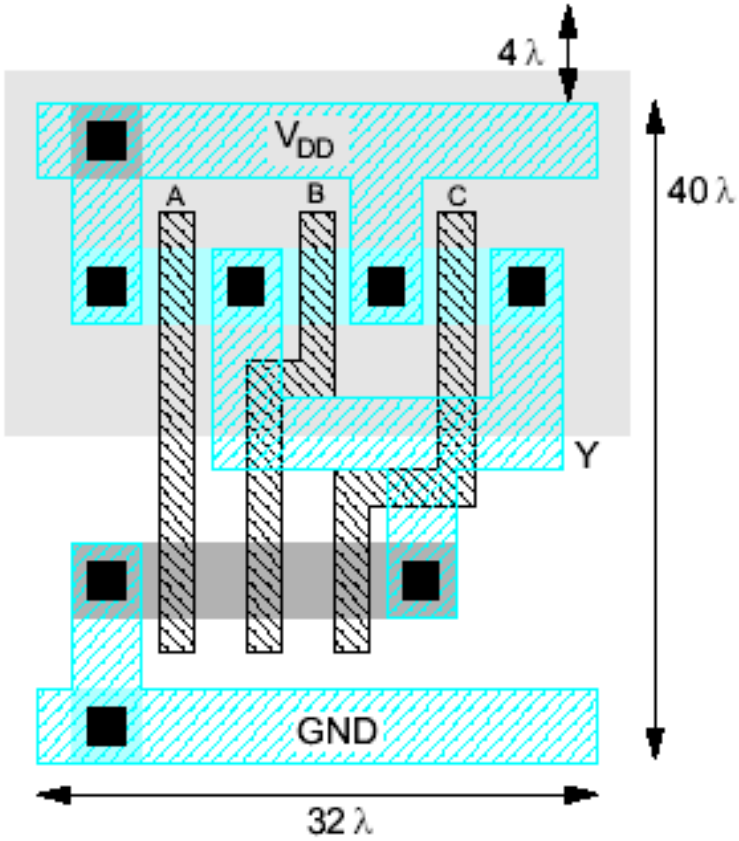
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



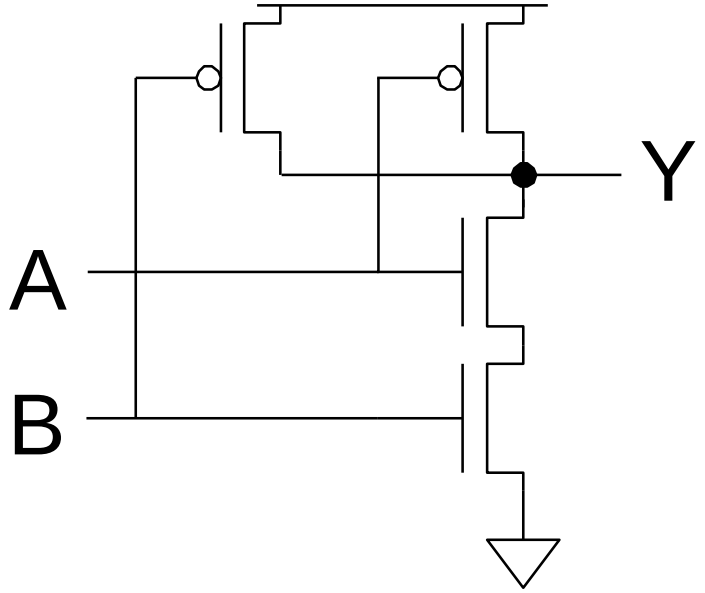
Example: NAND3

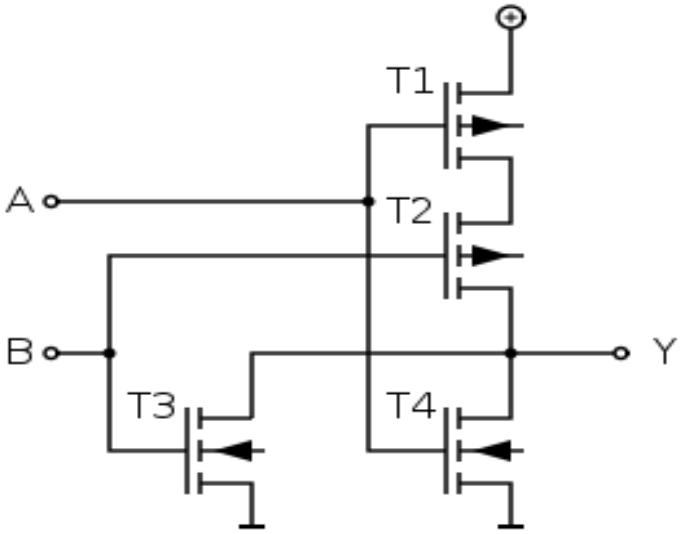
- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



Sarcina tehnică la proiectul de an la disciplina „TPS VLSI”

De calculat dimensiunile și parametrii tranzistorilor, de simulat schema electrică principială ce conține elementele CMOS, de elaborat topologia circuitului integrat, de elaborat construcţia măştilor pentru realizarea circuitului şi de descris fişa tehnologică în corespundere cu tehnologiile avansate CMOS, de prezentat vederea în secțiune a tranzistorilor și elementelor CMOS. De prezentat fișierul de verificare a schemei și de testat circuitele elaborate.





Datele iniţiale pentru proiect:

1. Schema de principiu al circuitului constă din **X** elemente Și-Nu/ Sau - Nu
2. Coeficientul de ramificare $K_{ram} = 9$
3. Capacitatea sarcinii $C_s = 6$ pF
4. Timpul de reţinere $t_{reț} = 5$ ns
5. Tensiunea sursei de alimentare $U_{s.a.} = 9$ V
6. Tensiunea „0” logic de ieşire $U_{ieș}^{0} = 0{,}65$ V
7. Tensiunea „1” logic de ieşire $U_{ieș}^{1} = 6.5$ V
8. Rezerve de stabilitate la perturbaţii $U_{pert} = 0{,}75$ V
9. Concentraţia impurităţilor în plachetă $N_0^n = 2 \cdot 10^{15}$ cm^{-3}
10. Concentraţia impurităţilor în regiunea *p* $N_0^p = 3 \cdot 10^{16}$ cm^{-3}
11. Concentraţia stărilor de suprafaţă $N_{supr} = 3 \cdot 10^{11}$ cm^{-2}
12. Mobilitatea electronilor $\mu_n = 470$ cm^2/(V·s)
13. Mobilitatea golurilor $\mu_p = 190$ cm^2/(V·s)
14. Diapazonul temperaturii de funcţionare T = -30 ˚C - +45 ˚C
15. Materialul grilei „poli Si”
16. Tehnica „LOCOS”

Calculam tensiunea de prag necesara pentru tranzistorul unipolar $|U_0|$ pentru acordarea rezervei de stabilitate la perturbatii date dupa formula, in conditiile $U_{int}^0 = U_{ieș}^0$ si $U_{int}^1 = U_{ieș}^1$.

$$\mathbf{U_{pert}} = \begin{cases} (\mathbf{U_0} - \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_1}) - \mathbf{U_{ies}^0} \\ \mathbf{U_{ies}^1} - (\mathbf{U_0} + \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_2}) \end{cases}. \qquad \boldsymbol{U_{по}} = \boldsymbol{min} \begin{cases} \boldsymbol{U_{пом}^+} = \boldsymbol{min} \begin{cases} (\boldsymbol{U_0} - \boldsymbol{TKU_0}\Delta\boldsymbol{T_1}) - \boldsymbol{U_{вх}^0} \\ \boldsymbol{U_{вх}^1} - (\boldsymbol{U_0} + \boldsymbol{TKU_0}\Delta\boldsymbol{T_2}) \end{cases} \\ \boldsymbol{U_{пом}^-} \end{cases}$$

$\mathrm{T}\mathbf{KU_0}$ – coieficientul temperaturii tensiunilor de prag (~ 4 mV/°C); $\Delta\mathrm{T_1} = \mathrm{T_{max}} - \mathbf{T_{cam}}$; $\Delta\mathrm{T_2} = \mathbf{T_{cam}} - \mathrm{T_{min}}$; $\mathbf{T_{cam}} = +20$°C.

$$\Delta\mathrm{T_1} = \mathrm{T_{max}} - \mathbf{T_{cam}} = 45\text{°C} - 20\text{°C} = 25\text{°C}.$$

$$\Delta\mathrm{T_2} = \mathbf{T_{cam}} - \mathrm{T_{min}} = 20\text{°C} - (-30\text{°C}) = 50\text{°C}.$$

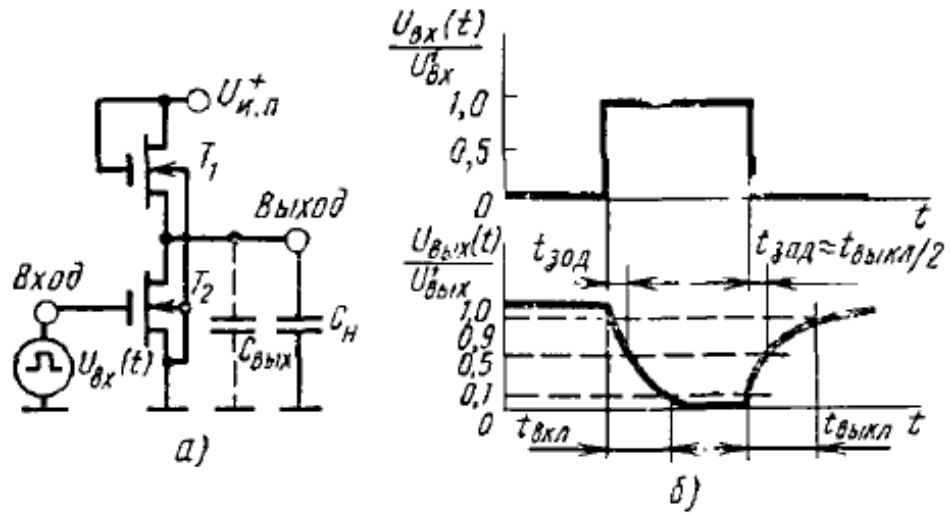


Рис. 2.16. Схема включения (*а*) и временные диаграммы работы инвертора (*б*) в динамическом режиме

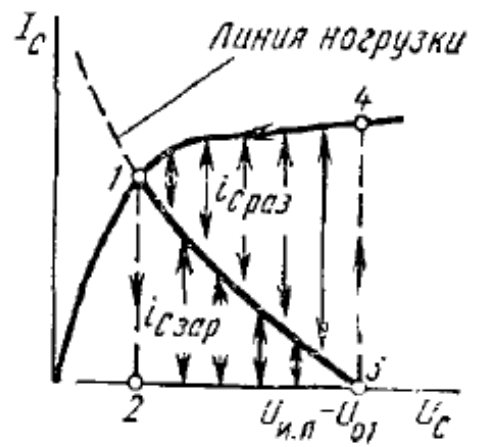


Рис. 2.17. К определению быстродействия инвертора

$$\mathbf{U_{pert}} = \begin{cases} (\mathbf{U_0} - \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_1}) - \mathbf{U_{ies}^0} \\ \mathbf{U_{ies}^1} - (\mathbf{U_0} + \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_2}) \end{cases} \Rightarrow \begin{cases} \mathbf{U_{pert}} = (\mathbf{U_0} - \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_1}) - \mathbf{U_{ies}^0} \\ \mathbf{U_{pert}} = \mathbf{U_{ies}^1} - (\mathbf{U_0} + \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_2}) \end{cases} \Rightarrow$$

$$\begin{cases} \mathbf{U_0} = \mathbf{U_{pert}} + \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_1} + \mathbf{U_{ies}^0} \\ \mathbf{U_0} = \mathbf{U_{ies}^1} - \mathbf{U_{pert}} - \mathrm{T}\mathbf{KU_0}\Delta\mathrm{T_2} \end{cases} \Rightarrow \begin{cases} \mathbf{U_0} = \mathbf{0,75V} + \frac{\mathbf{4mV}}{\mathrm{°C}} * \mathbf{25}\mathrm{°C} + \mathbf{0,65V} = \mathbf{1,5V} \\ \mathbf{U_0} = \mathbf{6.5V} - \mathbf{0,75V} - \frac{\mathbf{4mV}}{\mathrm{°C}} * \mathbf{50}\mathrm{°C} = \mathbf{5,55V} \end{cases}.$$

$$\begin{cases} \mathbf{U_0} = \mathbf{1,5V} \\ \mathbf{U_0} = \mathbf{5,55V} \end{cases}.$$

Determinăm capacitatea specifica a porții relative canalului $C_{з0}$ pentru tranzistoare p- si n-canale după formule, cu condiția $\varphi_{мп} = 0$.

$$\varepsilon_0 = 8{,}854 \cdot 10^{-12} \left[\frac{F}{m}\right] = 8{,}854 \cdot 10^{-14} \left[\frac{F}{cm}\right]$$

$$\varepsilon_{п} = 11.7 \left[\frac{F}{m}\right] = 11.7 \cdot 10^{-2} \left[\frac{F}{cm}\right]$$

$\varphi_T \sim 0{,}026\ V$

$n_i = 2 * 10^{10}\text{см}^{-3}$

Pentru *n- canal:* $\varphi\phi_i = \varphi_T ln(N_0/n_i) = 0.26 * \ln\left(\frac{3*10^{15}}{2*10^{10}}\right) = 0.309V$

Pentru *p-canal:* $\varphi\phi_i = \varphi_T ln(N_0/n_i) = 0.26 * \ln\left(\frac{4*10^{15}}{2*10^{10}}\right) = 0.377V$

$$Q_{SS} = q * N_{пов} = 1{,}6 \cdot 10^{-19} C \cdot 4 \cdot 10^{11} cm^{-2} = 6{,}4 * 10^{-8}\ C/cm^2$$

$$Q_{пп} = \sqrt{2\varepsilon_0 \varepsilon_п N_0 \varphi \phi_i q} = \sqrt{2 \cdot 8{,}854 \cdot 10^{-14} \cdot 11.7 \cdot 10^{-2} \cdot 3 \cdot 10^{15} \cdot 0{,}309 \cdot 1{,}6 \cdot 10^{-19}} = 1{,}75 \cdot 10^{-9} C/cm^2$$

$$Q_{пр} = \sqrt{2\varepsilon_0 \varepsilon_п N_0 \varphi \phi_i q} = \sqrt{2 \cdot 8{,}854 \cdot 10^{-14} \cdot 11.7 \cdot 10^{-2} \cdot 4 \cdot 10^{16} \cdot 0{,}377 \cdot 1{,}6 \cdot 10^{-19}} = 7{,}07 \cdot 10^{-9} C/cm^2$$

$$\mathbf{U_0 = -\left(\left|\varphi_{mp}\right| + \frac{Q_{SS}}{C_{z0}} + \frac{Q_p}{C_{z0}} + 2\varphi\Phi_i\right) = -\frac{Q_{SS}}{C_{z0}} - \frac{Q_p}{C_{z0}} - 2\varphi\Phi_i = -\frac{Q_{SS} + Q_p}{C_{z0}} - 2\varphi\Phi_i \Rightarrow}$$

$$\mathbf{C_{z0} = \frac{Q_{SS}+Q_p}{U_0+2\varphi\Phi_i} = \frac{4.8*10^{-8}\frac{C}{cm^2}+61*10^{-8}\frac{C}{cm^2}}{1.5V+0.74V} = 2.93 * 10^{-7} F/cm^2.}$$

$$\boldsymbol{U_0 = -\left|\varphi_{mp}\right| - \frac{Q_{SS}}{C_{z0}} + \frac{Q_p}{C_{z0}} + 2\varphi\Phi_i}$$ **(pentru tranzistor n-canal).**

$$\boldsymbol{U_0 = -\left|\varphi_{mp}\right| - \frac{Q_{SS}}{C_{z0}} + \frac{Q_p}{C_{z0}} + 2\varphi\Phi_i = -\frac{Q_{SS}}{C_{z0}} + \frac{Q_p}{C_{z0}} + 2\varphi\Phi_i = \frac{Q_p - Q_{SS}}{C_{z0}} + 2\varphi\Phi_i \Rightarrow}$$

$$\boldsymbol{C_{z0} = \frac{Q_p - Q_{SS}}{U_0 - 2\varphi\Phi_i} = \frac{\left|15 * 10^{-8}\frac{C}{cm^2} - 4.8 * 10^{-8}\frac{C}{cm^2}\right|}{1.5V - 0.6V} = 1.13 * 10^{-7} F/cm^2.}$$

$$\boldsymbol{C_{z0} = 2.93 * 10^{-7} F/cm^2}$$ **– p tip.**

$$\boldsymbol{C_{z0} = 1.13 * 10^{-7} F/cm^2}$$ **– n tip.**

Gasim grosimea dielectricului din poarta h_d dupa formula pentru structurilei p- si n-canal si se alege valoarea mai mare.

$$C_{z0} = \frac{\varepsilon_0 \varepsilon_d}{d} \Rightarrow h_d = \frac{\varepsilon_0 \varepsilon_d}{C_{z0}}.$$

$$h_Д = max \begin{cases} h_Д^p = \frac{\varepsilon_0 \varepsilon_Д}{C_{з0}} = \frac{8{,}85*10^{-14}*3{,}9}{3.33*10^{-8}} = \frac{3.45 \cdot 10^{-13}}{3.33*10^{-8}} = 1.03 \cdot 10^{-5} = 0{,}103\ \mu m \\ h_Д^n = \frac{\varepsilon_0 \varepsilon_Д}{C_{з0}} = \frac{8{,}85*10^{-14}*3{,}9}{8.16*10^{-8}} = \frac{3.45 \cdot 10^{-13}}{8.16*10^{-8}} = 4.22 \cdot 10^{-5} = 0{,}422 \mu m \end{cases}$$

$$h_Д = 0{,}422 \mu m$$

Verificarea condiției pentru valoarea selectată a grosimii dielectricului porții h_d.

$$U_{s.a.} > |U_{01}| + U_{02} \Rightarrow 9V > 1{,}5V + 5{,}55V \Rightarrow 9V > 7{,}05V.$$

Calculam lungimea tehnologica a canalului tranzistorului de incarcare (l_{k1tehn}) si tranzistorului cheie (l_{k2tehn}) dupa Tabelul.3.1 si formula.

$$l_{k.tehn.} = l_z - 2i = 5\mu m - 2 * 1\mu m = 3\mu m.$$

$$l_{k.tehn.} = 3\mu m.$$

Calculam panta specifica S_{01} tranzistorului de incarcare dupa formule cu conditiile date C_s si t_{off} =2 t_{ret} in dependent de schema invertorului.

$$K = \frac{(U_{s.a.} - U_0)}{U_{s.a.}} = \frac{(9V - 1{,}5V)}{9V} = 0{,}83.$$

t_{off} =2 t_{ret} = 2*5 ns = 10 ns. 0.000105

$$t_{выкл} = \frac{C_н}{S_{01}(U_{и.п.} - U_0)} \left[ln(20K - 1) + \frac{0{,}9 - K}{0{,}5K} \right]$$

$$t_{off} = \frac{C_s}{S_{01}(U_{s.a.} - U_0)} \left[ln(20K - 1) + \frac{0,9 - K}{0,5K} \right] \Rightarrow S_{01} = \frac{C_s[ln(20K - 1) + \frac{0,9 - K}{0,5K}]}{t_{off}(U_{s.a.} - U_0)}$$

$$= \frac{6 * 10^{-12} \left(log(20 * 0.85 - 1) + \frac{0.9 - 0.85}{0.5 * 0.85} \right)}{10 * 10^{-9} * (9 - 1,5)} = 1.9 * 10^{-4} A/B^2.$$

Calculam panta specifica S_{02} tranzistorului de incarcare dupa formule cu conditiile date Cs si t_{off} =2 t_{ret} in dependent de schema invertorului.

$$S_{02} = \frac{C_s[ln(20K - 1) + \frac{0,9 - K}{0,5K}]}{t_{off}(U_{s.a.} - U_0)} = \frac{6 * 10^{-12}(log(20 * 0.85 - 1) + \frac{0.9 - 0.85}{0.5 * 0.85})}{10 * 10^{-9} * (9 - 5.55)}$$

$$= 4.1 * 10^{-4} A/B^2.$$

8) Găsim relația dintre lățimea canalului tranzistorului de încărcare si celui cheie la lungimea lui $b_{к1}/l_{к1техн}$ si $b_{к2}/l_{к2техн}$ după formula $S_0 = \mu C_{з0} b_к / l_к$ cu conditiile date ale mobilitatii purtatorilor de sarcina μ_n si μ_p.

$$S_0 = \frac{\mu C_{з0} b_к}{l_к} \Rightarrow \frac{b_к}{l_к} = \frac{S_0}{\mu C_{з0}}$$

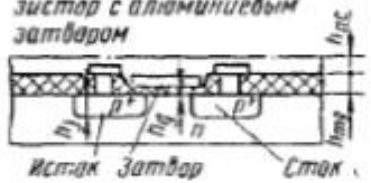
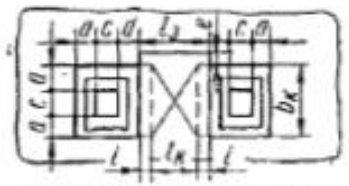
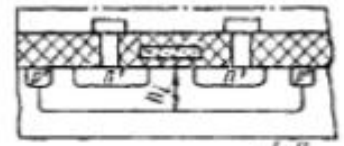
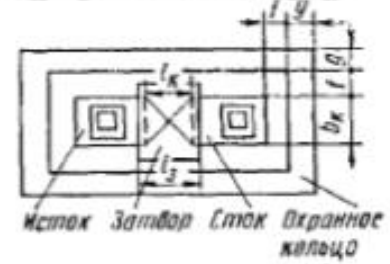
$$(p) \quad \frac{b_{к1}}{l_{к1техн}} = \frac{S_{01}}{\mu_p C_{з0}} = \frac{0.714 * 10^{-4}}{200\, {cm^2}/{Vs} * 3.33 * 10^{-8} F/cm^2} = 10.72$$

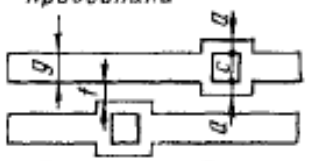
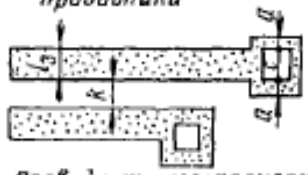
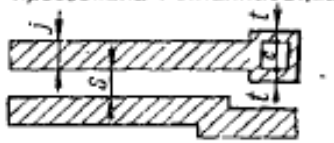
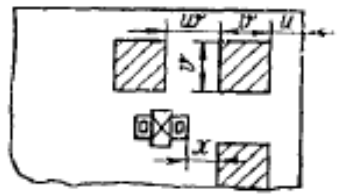
$$(n) \quad \frac{b_{к2}}{l_{к2техн}} = \frac{S_{02}}{\mu_n C_{з0}} = \frac{1{,}42 * 10^{-4}}{450\, {cm^2}/{Vs} * 8.16 * 10^{-8} F/cm^2} = 3.86$$

$$(p) \quad b_{к1} = l_{к1техн} * 10.72 = 3\mu m * 10.72 = 32.6\ \mu m$$

$$(n) \quad b_{к1} = l_{к1техн} * 3.86 = 3\mu m * 3.86 = 11.58\mu m$$

Технологические ограничения на размеры МДП-структур

Чертежи топологии	Наименование элемента топологии, наименование и обозначение размера	Вид технологии		
		p-МДП	n-МДП	КМДП
p-канальный МДП-транзистор с алюминиевым затвором  	Толщина затворного диэлектрика (SiO_2) $h_д$, мкм	0,07—0,10	0,07—0,1	⩾0,1
	Толщина толстого диэлектрика (SiO_2) $h_{тд}$, мкм	1,0	1,0	1,0
	Толщина металлизации (алюминия) $h_м$, мкм	1,2	1,2	1,2
	Толщина кремниевого затвора $h_{з.к.з}$, мкм	—	0,5	0,5
	Толщина межслойной изоляции (ФСС) $h_{м.и}$, мкм	—	1,0	1,0
	Толщина пассивирующего слоя (ФСС) $h_{пс}$, мкм	1,0	1,0	1,0
	Толщина стоков, истоков, диффузионных проводников h_j, мкм	1,5	1,0	1,0 (n^+) 1,5 (p^+)
	Толщина p-областей для формирования n-канальных транзисторов КМДП-ИМС h_t, мкм	—	—	6,0—7,0
	Минимальная длина алюминиевого (кремниевого) затвора l_2, мкм	12	5	5
	Перекрытие областей стока (истока) алюминиевым (кремниевым) затвором i, мкм	2,0	0,8	1,0
n-канальный МДП-транзистор с кремниевым затвором 	Минимальное расстояние от края контактного окна до края стока (истока), диффузионного проводника, кремниевого затвора a, мкм	4,0	2,0	2,0
	Минимальный размер контактного окна к стоку (истоку), диффузионному проводнику и кремниевому затвору $c \times c$, мкм	6×6	5×5	5×5
	Минимальное расстояние от затвора до края контактного окна к стоку (истоку) d, мкм	10,0	4,0	4,0
 	Перекрытие области канала затвором на его конце e, мкм	3,0	2,0	До охранного кольца (Al) 2,0 (Si)
	Минимальное расстояние между соседними стоковыми (истоковыми) областями и диффузионными проводниками f, мкм	10,0	5,0	5,0

Чертежи топологии	Наименование элемента топологии, наименование и обозначение размера	Вид технологии		
		p-МДП	*n*-МДП	КМДП
Диффузионные проводники 	Минимальная ширина диффузионного проводника и охранного кольца g, мкм	8,0	5,0	5,0
	Минимальное расстояние между кремниевыми затворами k, мкм	—	4,0	4,0
	Минимальное расстояние между алюминиевыми затворами и между проводниками металлизации s, мкм	8,0	5,0	5,0
Поликремниевые проводники 	Минимальная ширина проводников металлизации j, мкм	8,0	5,0	5,0
	Перекрытие проводником металлизации контактного окна ко всем областям t, мкм	3,0	2,0	2,0
Проводники металлизации 	Расстояние от края кристалла до контактной площадки u, мкм		$\geqslant 50$	
	Минимальный размер контактной площадки для ручной (числитель) и автоматизированной (знаменатель) термокомпрессионной сварки $v \times v$, мкм		$\frac{50 \times 50}{150 \times 150}$	
Контактные площадки 	Минимальное расстояние между контактными площадками для ручной (числитель) и автоматизированной (знаменатель) термокомпрессионной сварки w, мкм		$\frac{70}{50}$	
	Расстояние между контактными площадками и другими элементами схемы x, мкм		20	

9) Determinăm alți parametri constructivi ale tranzistorilor de încărcare și celor cheie, inelelor de securitate, diodelor după tabelul 3.1 luând in considerație recomandările anterioare.

- Grosimea dielectricului pe poarta $h_{Д} = 0{,}42\ um$
- Grosimea dielectricului lat $h_{ТД} = 1\ um$
- Grosimea metalizării (aluminiului) $h_{м} = 1{,}2\ um$
- Grosimea porții din Si $h_{п.к.з} = 0{,}5\ um$
- Grosimea izolării intre straturi $h_{м.и} = 1\ um$
- Grosimea stratului de pasivare $h_{пс} = 1\ um$
- Grosimea surselor, drenelor, conductorilor difuzați $h_j = 1um(9+),\ 1{,}5um(n+)$
- Grosimea p – regiunilor pentru formarea tranzistorilor n – canal $h_i = 6\ um$
- Lungimea minimala porții din aluminiu (siliciu) $l_з = 12$ мкм (p), $l_з = 5\ um$ (n)
- Suprapunerea zonelor drenei (sursei) cu poarta din aluminiu (siliciu) $i = 2\ um$ (p), $i = 0.8\ um$ (n)
- Distanța minimă de la marginea ferestrei de contact până la marginea drenei (sursei), conductorului difuzat, porții din siliciu $a = 4\ um$ (p), $a = 2\ um$ (p)
- Distanța minimă de la marginea a ferestrei de contact la drena (sursa), conductorul difuzat si poarta din siliciu $c * c = 6 * 6\ um$ (p), $c * c = 5 * 5\ um$ (n)
- Distanța minimă de la poarta la marginea ferestrei de contact la drena (sursa) $d = 10\ um$ (p), $d = 4\ um$ (n)

- Suprapunerea zonei canalului cu poarta la marginea lui $e = 3\ um\ (Si)$ (p), $e = 2\ um\ (Si)$ (n)
- Distanța minimă intre zonele drenei (sursei) din vecinătate si conductorilor difuzați $f = 10\ um$ (p), $f = 5\ um$ (n)
- Lățimea minimala conductorului difuzat si inelului de securitate $g = 8um$ (p), $g = 5um$ (n)
- Distanța minimă dintre porțile din siliciu $k = 4\ um$ (n)
- Distanța minimă dintre porțile de aluminiu si conductorilor metalizați $s = 5\ um$ (n), $s = 5\ um$ (n)
- Lătimea minimă a conductorilor metalizați $j = 8\ um$ (n), $j = 5\ um$ (n)
- Suprapunerea cu conductorul metalizat a ferestrei de contact la toate zonele $t = 3\ um$ (n), $t = 2\ um$ (n)
- Distanta de la marginea cristalului până la suprafața de contact $u \geq 50\ um$
- Dimensiunea minima a suprafeței de contact pentru sudarea termocompresionistă (numitor) si automata (numarator) $v * v = (50 * 50)/\ (150 * 150)\ um$
- Distanta minima dintre contactele suprafetei pentru sudarea termocompresionista (numitor) si automata (numerator) $w = 70/50\ um$
- Distanta intre contactele suprafeței si alte elemente a schemei $x = 20\ um$