Laboratory work Nr 2

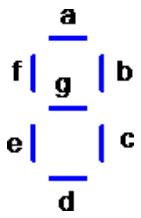
BCD to 7 segment decoder

Purpose

The purpose of this laboratory work is to design and implement combinatorial logic that will decode a 4-bit BCD input to a seven segment LED display.

INTRODUCTION

A seven-segment decoder is a logic circuit often used for the visual display of digital information. The seven outputs of the decoder will drive the seven segments on a corresponding display. BCD is the acronym for Binary Coded Decimal. The BCD system is used to represent the decimal numbers from 0 to 9 in a binary format suitable for digital devices. A four-bit code is required with the decimal characters 0 through 9 represented by the binary numbers 0000 through 1001. The combinations 1010 through 1111 are not used. A BCD to seven-segment decoder will allow the display of a binary coded decimal on a seven-segment display. The input to the decoder is a number from 0 through 9 in BCD and the output provides the seven inputs required to drive the seven-segment display.



Task

1. Create the truth table describing the function of a BCD to seven-segment decoder according to your variant (Table 1). The lower case letters, a-g, represent the segments on the display while x1, x2, x3 and x4 represent the BCD input. Observe that x4 is the least-significant bit of the BCD input.
2. After completing the truth table, make Karnaugh-map for each of the seven outputs. Reduce the Karnaugh maps to obtain a minimal sum expression for each segment.
3. Find common terms for minimal sum expressions and rewrite the formulas.
4. Design the circuit for the 7 segment decoder in Logic Works
   Note: Use NAND gates to implement the circuit.

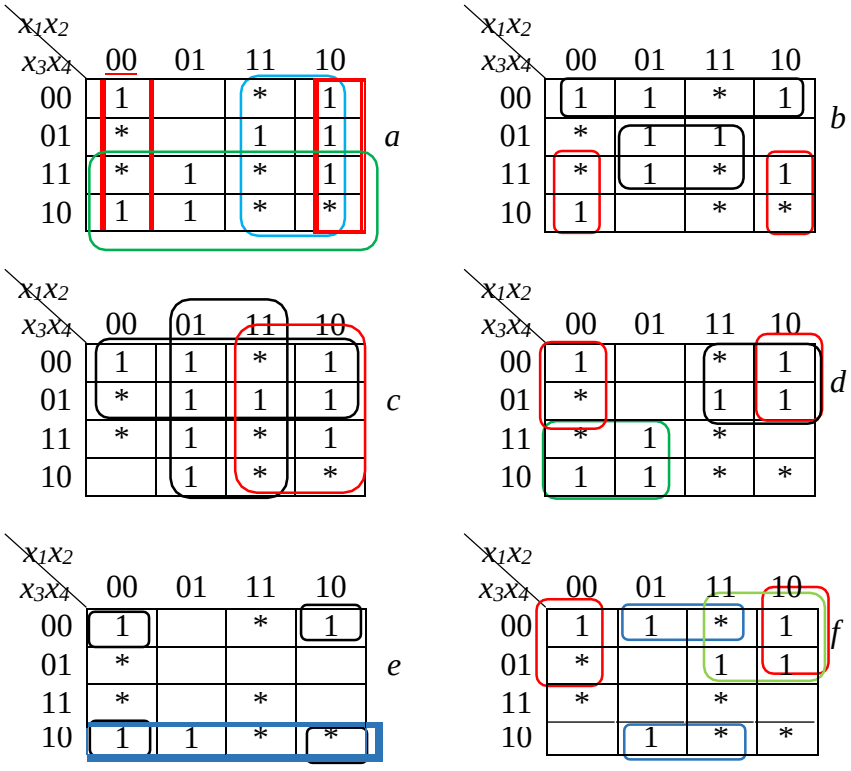
Table 1

No	BCD
1.	8 7 (-2)(-4)
2.	8 6 (-1)(-4)
3.	8 5 (-2)(-4)
4.	8 4 3 (-6)
5.	8 6 1 (-4)
6.	8 5 2 (-4)
7.	8 4 3 (-2)
8.	8 4 2 1+3
9.	8 4 2 (-1)
10.	8 4 2 1+6
11.	8 4 1 (-2)
12.	8 3 2 (-4)
13.	8 4 2 (-5)
14.	8 4 1 (-6)
15.	8 4 1 (-2)
16.	5 3 2 (-1)
17.	5 3 1 (-1)
18.	3 3 2 1
19.	4 2 2 1
20.	4 3 1 1
21.	4 3 2 (-1)
22.	4 3 2 1
23.	4 4 1 (-2)
24.	4 4 2 (-1)
25.	4 4 3 (-2)
26.	4 4 2 1
27.	5 2 1 1
28.	5 2 2 (-1)
29.	5 3 2 (-1)
30.	5 2 2 1

Example of implementation.

Implement a 8423 to 7-segment decoder using NAND gates

Decimal digit	BCD 8 x_1	4 x_2	2 x_3	-3 x_4	7 segment decoder outputs a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	1	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	1	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	1	0	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	1	0	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	1	0	1	1	1	1	1	0	1	1
	0	0	0	1	*	*	*	*	*	*	*
	0	0	1	1	*	*	*	*	*	*	*
	1	0	1	0	*	*	*	*	*	*	*
	1	1	0	0	*	*	*	*	*	*	*
	1	1	1	0	*	*	*	*	*	*	*
	1	1	1	1	*	*	*	*	*	*	*



x_3x_4 \ x_1x_2	00	01	11	10
00		1	*	1
01	*		1	1
11	*	1	*	
10	1	1	*	*

g

Logic expressions

$$a = x_1 + \overline{x_2} + x_3 = \overline{\overline{x_1} \wedge x_2 \wedge \overline{x_3}}$$

$$b = \overline{x_3}\,\overline{x_4} + x_2x_4 + \overline{x_2}x_3 = \overline{\overline{x_3}\,\overline{x_4} \wedge \overline{x_2x_4} \wedge \overline{\overline{x_2}x_3}}$$

$$c = x_1 + x_2 + \overline{x_3} = \overline{\overline{x_1} \wedge \overline{x_2} \wedge x_3}$$

$$d = \overline{x_2}\,\overline{x_3} + x_1\overline{x_3} + \overline{x_1}x_3 = \overline{\overline{\overline{x_2}\,\overline{x_3}} \wedge \overline{x_1\overline{x_3}} \wedge \overline{\overline{x_1}x_3}}$$

$$e = \overline{x_2}\,\overline{x_4} + x_3\overline{x_4} = \overline{\overline{\overline{x_2}\,\overline{x_4}} \wedge \overline{x_3\overline{x_4}}}$$

$$f = \overline{x_2}\,\overline{x_3} + x_1\overline{x_3} + x_2\overline{x_4} = \overline{\overline{\overline{x_2}\,\overline{x_3}} \wedge \overline{x_1\overline{x_3}} \wedge \overline{x_2\overline{x_4}}}$$

$$g = x_1\overline{x_3} + x_2\overline{x_4} + \overline{x_1}x_3 = \overline{\overline{x_1\overline{x_3}} \wedge \overline{x_2\overline{x_4}} \wedge \overline{\overline{x_1}x_3}}$$

Common terms:

$$Z = \overline{\overline{x_2}\,\overline{x_3}}$$

$$Y = \overline{x_1\overline{x_3}}$$

$$W = \overline{\overline{x_1}x_3}$$

$$V = \overline{x_2\overline{x_4}}$$

Rewrited logic expressions:

$$a = x_1 + \overline{x_2} + x_3 = \overline{\overline{x_1} \wedge x_2 \wedge \overline{x_3}}$$

$$b = \overline{x_3}\,\overline{x_4} + x_2x_4 + \overline{x_2}x_3 = \overline{\overline{\overline{x_3}\,\overline{x_4}} \wedge \overline{x_2x_4} \wedge \overline{\overline{x_2}x_3}}$$

$$c = x_1 + x_2 + \overline{x_3} = \overline{\overline{x_1} \wedge \overline{x_2} \wedge x_3}$$

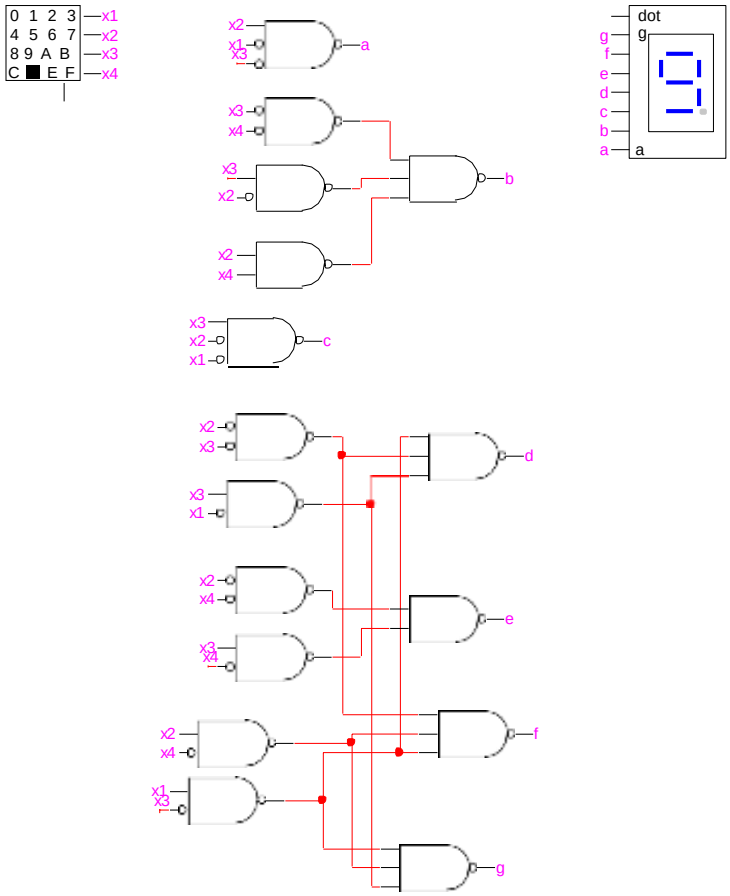
$$d = \overline{x_2}\,\overline{x_3} + x_1\overline{x_3} + \overline{x_1}x_3 = \overline{Y \wedge Z \wedge W}$$

$$e = \overline{x_2}\,\overline{x_4} + x_3\overline{x_4} = \overline{\overline{\overline{x_2}\,\overline{x_4}} \wedge \overline{x_3\overline{x_4}}}$$

$$f = \cancel{x_2\,\overline{x_3}} + \cancel{x_1\,\overline{x_3}} + \cancel{x_2\,\overline{x_4}} = \cancel{Z \wedge Y \wedge V}$$

$$\{ \quad g = x_1\overline{x_3} + x_2\overline{x_4} + \overline{x_1}x_3 = \overline{V \wedge Y \wedge W}$$

Logic circuit



Report

The report for the laboratory work will include:

1. Individual task according to the variant;
2. Truth table. Minimization of logic functions;
3. Rewritten logic expressions using common terms;
4. Designed logic circuits. Cost and delay time. Timing diagramm;
5. Captures of each decimal digit on 7 segment decoder.
6. Conclusions.